Small-Signal Modeling and Controller Design of a Grid-Connected Inverter for Solid State Transformer

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Approved by

Advisor
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Abstract

A single-phase grid-connected inverter for solid state transformer (SST) is presented. This work is aimed at the modeling and the design of control schemes for the inverter. In this thesis, a small-signal model for the grid-connected inverter with modified bipolar pulse width modulation method is developed. Small-signal analysis allows to predict the stability and dynamics of the inverter. Based on theoretical analysis, controllers are designed to improve dynamics and to guarantee stability of the system.

A high power factor and low harmonics are desirable in transmission system to improve the efficiency of the utility line. The current controller of the single-phase grid-connected inverter has sinusoidal reference to achieve power factor correction (PFC) and harmonics suppression. Proportional-integral (PI) scheme is widely used to control the power converter. The PI controller has the infinite gain at dc so it is suitable to track the dc reference. However, it is not good for tracking sinusoidal reference due to its finite gain at ac. The proportional-resonant (PR) controller which introduces large gain at specific frequency can track the sinusoidal reference without steady-state error but the error remains in step input response. The proportional-integral-resonant (PIR) controller has the advantage of both tracking the sinusoidal reference and removing the steady-state error for the step input. In this thesis, PIR controller is proposed for current control and design procedure for the PIR controller is presented.

In addition, the voltage controller is needed to regulate the dc link voltage. The voltage controller is designed to improve the audio-susceptibility and the output impedance characteristics. The dynamics and stability of the inverter system is analyzed. The proposed small-signal model and controllers are verified by PSIM simulation and experiments.

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List of Abbreviations

DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
PFC	Power Factor Correction
PI	Proportional-Integral
PIR	Proportional-Integral-Resonant
PR	Proportional-Resonant
PWM	Pulse Width Modulation
SST	Solid State Transformer
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

I. INTRODUCTION

Existing transformers for the ac power distribution system are efficient, reliable and durable, but its supply power quality totally depends on its input power quality because it cannot control power. And conventional transformers are bulky and heavy because they use the line frequency of 50 Hz or 60 Hz. Also they are related to environmental issues due to insulating oil [1], [2]. To solve these problems, solid state transformer (SST) is suggested as an alternative to conventional one. SST can reduce the size and weight of passive devices by increasing switching frequency of power switches above scores of kHz and can protect grid system when fault occurs in either grid or load [3]-[5]. In addition, allowing the bi-directional power flow, it helps renewable energy sources and electric vehicles in interfacing with the utility line [1], [6], [7].

Various ac-ac conversion structures for SST has been researched. Modular three-stage converter topology which is composed of bi-directional ac-dc inverters and a bi-directional isolated dc-dc converter is most promising due to its many attractive features [4]-[6]. To realize aforementioned functions, SST have to be properly controlled. For the high stability and the fast transient response, small-signal modeling is required before controller design. The small-signal model allows to predict system stability and dynamics with respect to various disturbances and perturbations. This thesis will focus on designing controllers for the single-phase grid-connected inverter based on the small-signal model.

Full-bridge topology which has simple circuit configuration is applied to the single-phase grid-connected inverter. In addition, it is most widely used due to its large power capacity and four quadrant operation. In the case of the full-bridge inverter, small-signal modeling of bipolar or unipolar pulse width modulation (PWM) method has been researched [8]-[11]. However, modified bipolar PWM method has not been studied. In this thesis, the small-signal model of the single-phase grid-connected inverter adopting modified bipolar PWM method is derived. The equivalent series resistance (esr) of an inductor and a capacitor is considered to more accurately predict stability and dynamic characteristics of the inverter system.

Harmonics of the current of the inverter has negative effects on a power grid, including deteriorating power quality by increasing total harmonic distortion (THD) of the grid voltage [12], [13]. Because they can cause many troubles in the grid, they are regulated by the rules. Also, it is required for the grid-connected inverter to make the inductor current in-phase with the grid voltage to reduce the reactive power. In order to achieve power factor correction (PFC) and harmonic suppression, current control strategies have been studied. Proportional-integral (PI) controllers are widely used for power converters. However, PI controllers present a steady-state error in inverter systems which have sinusoidal reference

[14], [15]. To overcome this problem, a proportional-resonant (PR) controller is applied to the inverter. The PR controller can provide large gain at the frequency of reference signal. Then, with the help of a resonant term, the PR controller can track the sinusoid without the steady-state error [14]-[18]. Although the PR controller is commonly used in single-phase inverter systems due to aforementioned merits, it presents steady-state error when reference signal has step change. This thesis proposes the proportional-integral-resonant (PIR) controller for single-phase inverters. The PIR controller enables to eliminate the steady-state error for the step input while tracking the sinusoidal reference.

In addition, the inverter is required to regulate the dc link voltage. The dc link may contain ripples including double line frequency ripples because the dc link voltage is the rectified utility line. The voltage controller is used to generate the constant dc link voltage. The PI controller provides infinite gain at dc (0 Hz). This thesis takes the advantage of the PI controller to track the constant reference of the voltage controller.

Regulating the dc link voltage and synchronizing the inductor current with the grid voltage are control goals of the bi-directional ac-dc inverter. The proposed small-signal model and controllers are verified by simulation and experimental results with the 3.3 kW single-phase grid-connected inverter prototype.

II. OPERATION PRINCIPLE AND SMALL-SIGNAL MODELING

This section presents small-signal modeling of the single-phase grid-connected inverter. Inverter control is challenging task because it has to control the dc link voltage and the inductor current simultaneously. In order to predict behavior of the inverter system, its accurate small-signal model is required. The small-signal model allows to analyze the stability and the dynamics of the inverter in frequency domain. Small-signal transfer functions can be derived using averaging, linearization and s-domain conversion. The validity of the derived mathematical model was verified by the given simulation results.

2.1 Operation Principle

This work uses the full-bridge topology for the inverter. Fig. 1 shows the basic circuit diagram of the single-phase grid-connected inverter system. The inverter consists of four power switches S_1-S_4, the filter inductor and the dc link capacitor. The filter inductor contains pure inductance L and esr r_l and the dc link capacitor contains pure capacitance C and esr r_c. It is assumed that other components excepting the inductor and the capacitor are ideal in the inverter circuit. Also, the voltage across the inductor and the capacitor are defined as v_L and v_{dc}, respectively, and current through the inductor and the capacitor are defined as i_L and i_C, respectively. Thus, constitutive equations for the inductor and capacitor can be described as follows.

$$\begin{cases} v_L(t) = L\dfrac{di_L(t)}{dt} + r_l i_L(t) \\ i_C(t) = C\dfrac{dv_{dc}(t)}{dt} - Cr_c\dfrac{di_C(t)}{dt} \end{cases} \tag{1}$$

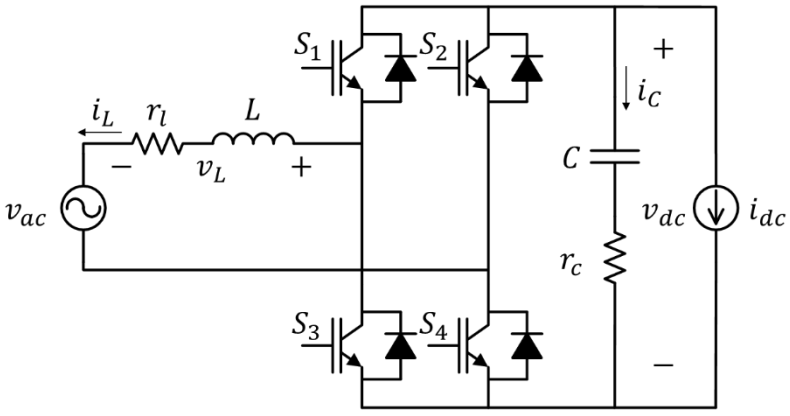
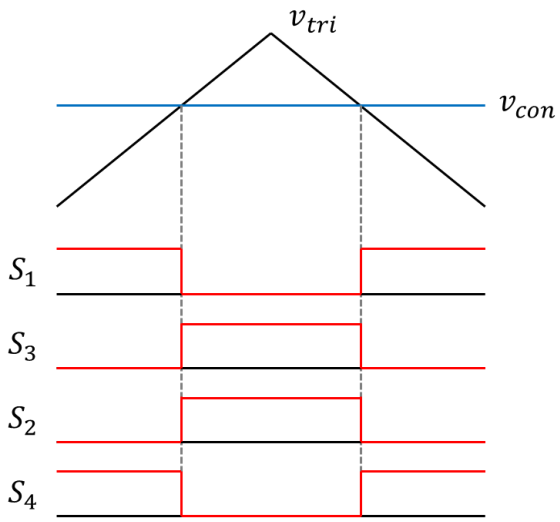


Fig. 1. Schematic diagram of the single-phase grid-connected inverter

Generally, bipolar PWM method and unipolar PWM method are used to control the inverter. In the case of bipolar PWM method, diagonal switches turn on or off simultaneously as shown in Fig. 2(a). So it is easy to implement. However, switching loss is high because all switches continue switching during the whole period. Unipolar PWM method, Fig. 2(b), has lower switching loss and EMI than bipolar PWM method but it is not inconsiderable.

Compared to conventional switching methodology, modified bipolar PWM method can reduce switching loss by using only two switches. Fig. 2(c) shows the modified bipolar PWM method that is applied to the inverter for the control. During half cycle of the grid voltage, two switches in one leg are complementally turned on or off by comparing the modulation signal v_{con} and triangular waveform v_{tri}. Otherwise, other two switches are not turned on and off. Therefore, the efficiency of the inverter increases. Also, it is clear that there are only two operation modes which are shown in Fig. 3(a) and Fig. 3(b).



(a)

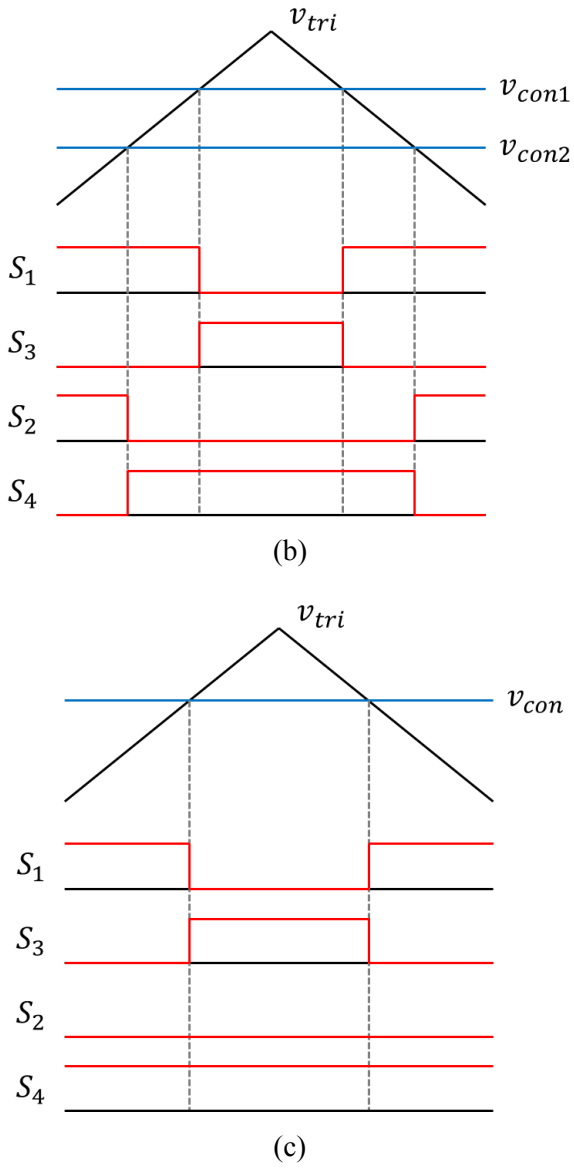


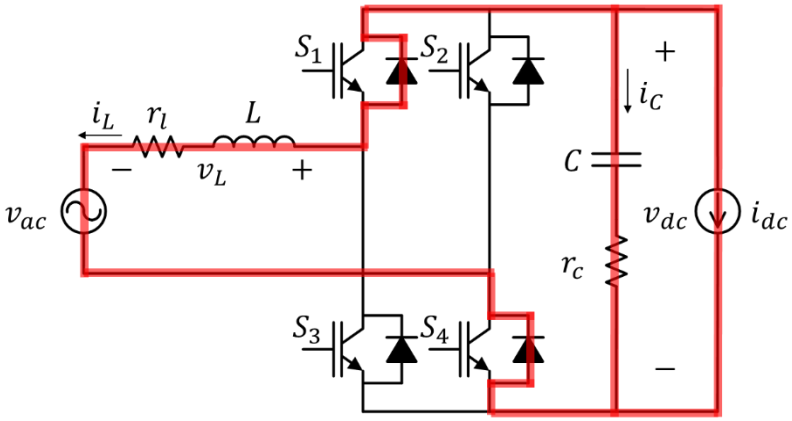
Fig. 2. PWM method (a) Bipolar PWM (b) Unipolar PWM (c) Modified bipolar PWM

During mode 1, as shown in Fig. 3(a), S_1 is in the on state and S_3 is in the off state. Based on Kirchhoff's law, the inductor voltage is the dc link voltage minus the grid voltage. The capacitor current is equal to the sum of the negative dc side current and the negative inductor current. Therefore, the following differential equations can be obtained for mode 1.

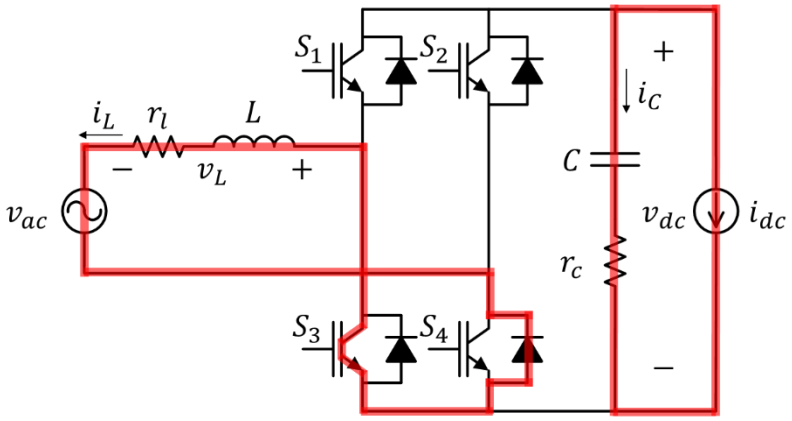
$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{v_{dc}(t)}{L} - \dfrac{v_{ac}(t)}{L} - \dfrac{r_l i_L(t)}{L} \\ \dfrac{dv_{dc}(t)}{dt} = -\dfrac{i_{dc}(t)}{C} - \dfrac{i_L(t)}{C} - r_c \dfrac{di_{dc}(t)}{dt} - r_c \dfrac{di_L(t)}{dt} \end{cases} \tag{2}$$

During the mode 2 in Fig. 3(b), S_1 is off and S_3 is on. Based on Kirchhoff's law, the inductor voltage is the negative grid voltage. The capacitor current is equal to the negative dc side current. Therefore, the following differential equations can be obtained for mode 2.

$$\begin{cases} \dfrac{di_L(t)}{dt} = -\dfrac{v_{ac}(t)}{L} - \dfrac{r_l i_L(t)}{L} \\ \dfrac{dv_{dc}(t)}{dt} = -\dfrac{i_{dc}(t)}{C} - r_c \dfrac{di_{dc}(t)}{dt} \end{cases} \tag{3}$$



(a)



(b)

Fig. 3. Operation modes (a) Mode 1 (b) Mode 2

2.2 Small-Signal Modeling

Through the averaging, linearization and conversion to s-domain step, the small-signal model of the inverter can be obtained. In the process of averaging, the time variance is removed. Time-varying inverter system is changed into time-invariant system.

In Fig. 2, when the triangular waveform frequency is much higher than modulation waveform frequency, switching function of switches can be averaged. The average value of the switching function becomes the duty ratio of switches. Using the duty ratio, (2) and (3) can be averaged as follows

$$\begin{cases} \dfrac{d\bar{\imath}_L(t)}{dt} = \dfrac{d(t)\bar{v}_{dc}(t)}{L} - \dfrac{\bar{v}_{ac}(t)}{L} - \dfrac{r_l\bar{\imath}_L(t)}{L} \\ \dfrac{d\bar{v}_{dc}(t)}{dt} = -\dfrac{\bar{\imath}_{dc}(t)}{C} - \dfrac{d(t)\bar{\imath}_L(t)}{C} - r_c\dfrac{d\bar{\imath}_{dc}(t)}{dt} - r_c d(t)\dfrac{d\bar{\imath}_L(t)}{dt} \end{cases} \tag{4}$$

where $d(t)$ is duty ratio of S_1 and the overbar denotes the average value over the switching period.

In the process of the linearization, the nonlinear relationship near the operating point is approximated to the linear relationship. All the state variables and input variables in (4) can be expressed as the sums of the dc component and the ac component

$$\begin{cases} v_{ac} = V_{ac} + \hat{v}_{ac} \\ i_{dc} = I_{dc} + \hat{\imath}_{dc} \\ d = D + \hat{d} \\ v_{dc} = V_{dc} + \hat{v}_{dc} \\ i_L = I_L + \hat{\imath}_L \end{cases} \tag{5}$$

where V_{ac}, I_{dc}, D, V_{dc} and I_L are dc components and $\hat{v}_{ac}$, $\hat{\imath}_{dc}$, $\hat{d}$, $\hat{v}_{dc}$ and $\hat{\imath}_L$ are ac components. It is assumed that ac components are much smaller than dc components. The dc components represent operating point and ac components represent small variation near the operating point.

By substituting (5) in (4) and solving for the dc components, the dc operating point is as follows:

$$\begin{cases} I_L = -\dfrac{I_{dc}}{D} \\ V_{dc} = \dfrac{DV_{ac} - r_l I_{dc}}{D^2} \end{cases} \tag{6}$$

By substituting (5) in (4) and solving for the ac components yields the following equations.

$$\begin{cases} \dfrac{d\hat{\imath}_L(t)}{dt} = \dfrac{D}{L}\hat{v}_{dc}(t) + \dfrac{V_{dc}}{L}\hat{d}(\mathrm{t}) - \dfrac{1}{L}\hat{v}_{ac}(t) - \dfrac{r_l}{L}\hat{\imath}_L(t) \\ \dfrac{d\hat{v}_{dc}(t)}{dt} = -\dfrac{1}{C}\hat{\imath}_{dc}(t) - \dfrac{D}{C}\hat{\imath}_L(t) - \dfrac{I_L}{C}\hat{d}(\mathrm{t}) - r_c\dfrac{d\hat{\imath}_{dc}(t)}{dt} - r_cD\dfrac{d\hat{\imath}_L(t)}{dt} - r_cI_L\dfrac{d\hat{d}(t)}{dt} \end{cases} \quad (7)$$

The small-signal transfer functions can be obtained using s-domain conversion. Laplace transform allows to convert time domain functions into frequency domain function and to analyze the system in respect to frequency. Using Laplace transform, (7) can be converted to (8).

$$\begin{cases} s\hat{\imath}_L(s) = \dfrac{D}{L}\hat{v}_{dc}(s) + \dfrac{V_{dc}}{L}\hat{d}(\mathrm{s}) - \dfrac{1}{L}\hat{v}_{ac}(s) - \dfrac{r_l}{L}\hat{\imath}_L(s) \\ s\hat{v}_{dc}(s) = -\dfrac{1}{C}\hat{\imath}_{dc}(s) - \dfrac{D}{C}\hat{\imath}_L(s) - \dfrac{I_L}{C}\hat{d}(\mathrm{s}) - sr_c\hat{\imath}_{dc}(s) - sr_cD\hat{\imath}_L(s) - sr_cI_L\hat{d}(s) \end{cases} \quad (8)$$

Based on the small-signal model, stability and dynamics of the inverter can be analyzed mathematically. Considering the small-signal dc link voltage and inductor current as the output variables, the inverter has six power stage transfer functions. There are the grid voltage-to-dc link voltage transfer function $G_{vs}(s)$, the grid voltage-to-inductor current transfer function $G_{is}(s)$, the dc side current-to-dc link voltage transfer function $Z_p(s)$, the dc side current-to-inductor current transfer function $Z_q(s)$, the duty ratio-to-dc link voltage transfer function $G_{vd}(s)$ and the duty ratio-to-inductor current transfer function $G_{id}(s)$. Each power stage transfer function is expressed as follows:

$$G_{vs}(s) = \frac{\hat{v}_{dc}(s)}{\hat{v}_{ac}(s)} = \frac{CDr_cs + D}{CLs^2 + (Cr_cD^2 + Cr_l)s + D^2} \quad (9)$$

$$G_{is}(s) = \frac{\hat{\imath}_L(s)}{\hat{v}_{ac}(s)} = -\frac{Cs}{CLs^2 + (Cr_cD^2 + Cr_l)s + D^2} \quad (10)$$

$$Z_p(s) = \frac{\hat{v}_{dc}(s)}{\hat{\imath}_{dc}(s)} = -\frac{CLr_cs^2 + (L + Cr_cr_l)s + r_l}{CLs^2 + (Cr_cD^2 + Cr_l)s + D^2} \quad (11)$$

$$Z_q(s) = \frac{\hat{\imath}_L(s)}{\hat{\imath}_{dc}(s)} = -\frac{CDr_cs + D}{CLs^2 + (Cr_cD^2 + Cr_l)s + D^2} \quad (12)$$

$$G_{vd}(s) = \frac{\hat{v}_{dc}(s)}{\hat{d}(s)} = -\frac{CI_LLr_cs^2 + (I_LL + CDV_{dc}r_c + CI_Lr_cr_l)s + V_{dc}D + I_Lr_l}{CLs^2 + (Cr_cD^2 + Cr_l)s + D^2} \quad (13)$$

$$G_{id}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{(CV_{dc} - CDI_L r_c)s - DI_L}{CLs^2 + (Cr_c D^2 + Cr_l)s + D^2} \quad (14)$$

Derived open-loop small-signal transfer functions of the inverter are verified using PSIM simulation. Circuit parameters used in simulation are listed in table 1.

TABLE I

CIRCUIT PARAMETERS FOR THE INVERTER

Parameter	Mark	Value
Grid voltage	v_{ac}	220 V_{rms}
Dc link voltage	v_{dc}	380 V
Filter inductance	L	1.601 mH
Equivalent series resistance of the inductor	r_l	391.2 mΩ
Dc link capacitance	C	2.272 mF
Equivalent series resistance of the capacitor	r_c	23.48 mΩ

Fig. 4-9 show the bode plot of each small-signal transfer function. Solid lines represent theoretical results obtained from the mathematical model and dotted lines represent ac sweep results obtained from PSIM simulation. The solid line is consistent with the dotted line below half the switching frequency. Near or above half the switching frequency, converter dynamics is affected by sampling effects and cannot be predicted using classical analysis.

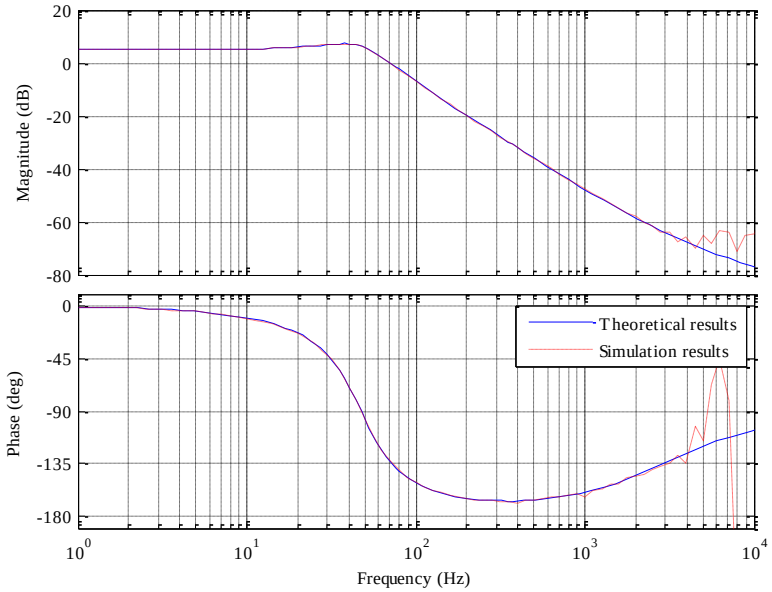


Fig. 4. Bode plot of the grid voltage-to-dc link voltage transfer function

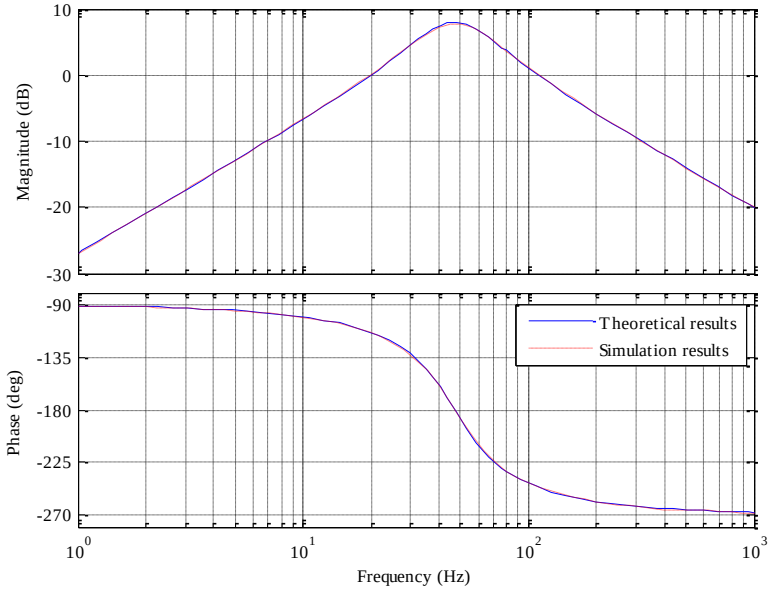


Fig. 5. Bode plot of the grid voltage-to-inductor current transfer function

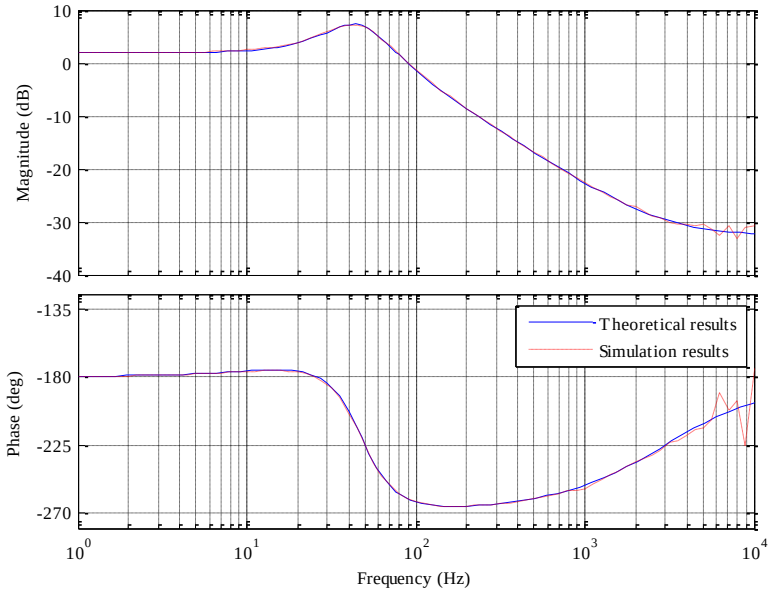


Fig. 6. Bode plot of the dc side current-to-dc link voltage transfer function

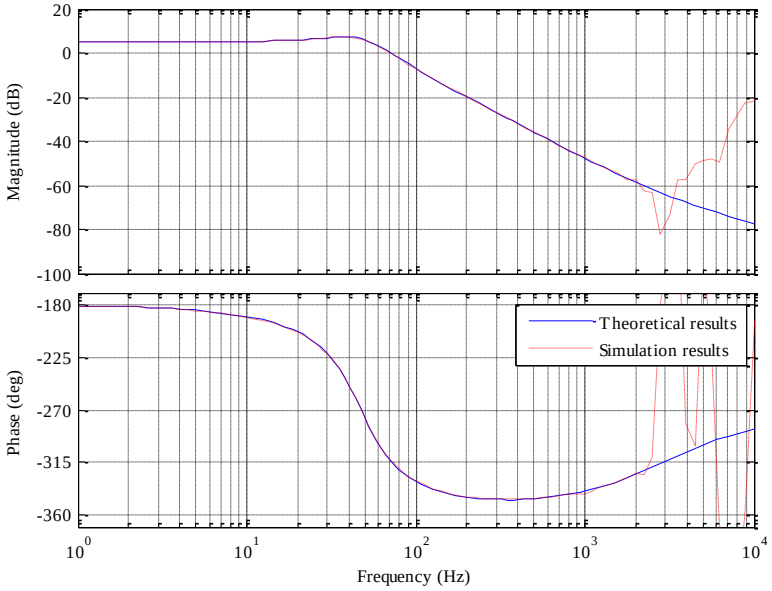


Fig. 7. Bode plot of the dc side current-to-inductor current transfer function

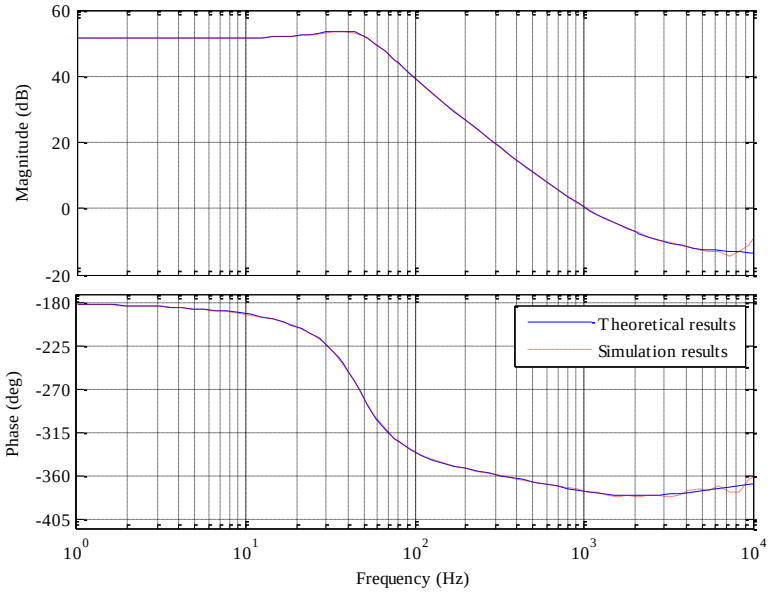


Fig. 8. Bode plot of the duty ratio-to-dc link voltage transfer function

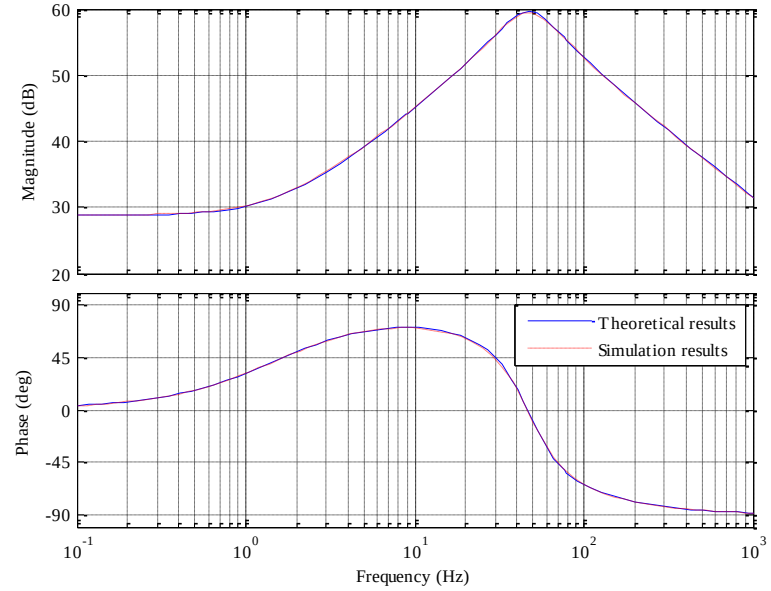


Fig. 9. Bode plot of the duty ratio-to-inductor current transfer function

III. CONTROLLER DESIGN

The inverter has two loops for control. One is the voltage loop regulating the dc link voltage and the other is the current loop achieving PFC and harmonic suppression. Based on the small-signal model, controllers are designed to obtain enough gain and phase margins and to improve the audio-susceptibility and the output impedance characteristics. The proposed small-signal model and controllers are validated using simulation and experimental results with the 3.3 kW single-phase grid-connected inverter prototype.

3.1 Current Controller Design

In this part, the current control principle and strategy are introduced. And new current controller is proposed to control the inverter current effectively. For design the current controller, the dc link voltage is assumed to be constant, i.e., the inverter operates as a voltage source inverter (VSI). Then (4) can be converted into (15).

$$si_L(\mathrm{s}) = \frac{V_{dc}}{L} d(s) - \frac{1}{L} v_{ac}(s) - \frac{r_l}{L} i_L(s) \tag{15}$$

Fig. 10(a) shows the block diagram of the VSI. The current reference $i_{ref}(s)$ is the product of $i_{mag}(s)$ and sine function. $G_{ci}(\mathrm{s})$ represents the current controller. The current loop gain of the VSI is defined as follows:

$$T_{vsi}(\mathrm{s}) = \frac{V_{dc}}{Ls + r_l} G_{ci}(\mathrm{s}) \tag{16}$$

As shown in Fig. 10(a), the inductor current can be expressed as follows:

$$i_L(\mathrm{s}) = \frac{T_{vsi}(\mathrm{s})}{1 + T_{vsi}(\mathrm{s})} i_{ref}(\mathrm{s}) - \frac{\frac{1}{Ls + r_l}}{1 + T_{vsi}(\mathrm{s})} v_{ac}(\mathrm{s}) \tag{17}$$

As shown in Fig. 10(b), with the aid of feed-forward control, the effect of the grid voltage on the inductor current can be removed. Feed-forward control block G_{ff} is the function of the dc link voltage.

$$G_{ff} = \frac{1}{V_{dc}} \tag{18}$$

Then, with feed-forward, the inductor current can be represented as

$$i_L(\mathrm{s}) = \frac{T_{vsi}(\mathrm{s})}{1 + T_{vsi}(\mathrm{s})} i_{ref}(\mathrm{s}) \tag{19}$$

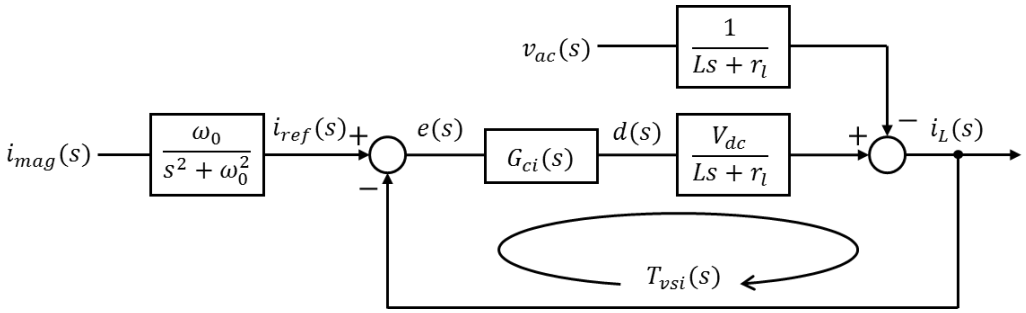
and the closed loop transfer function expression of the VSI is as follows:

$$G_{cl}(s) = \frac{i_L(s)}{i_{ref}(s)} = \frac{T_{vsi}(s)}{1 + T_{vsi}(s)} \tag{20}$$

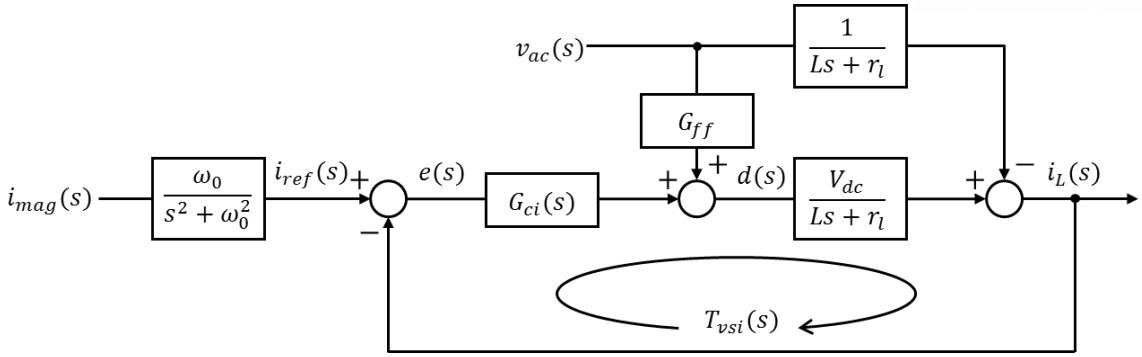
The error is defined as the difference between the reference current and the actual inductor current.

$$e(s) = i_{ref}(s) - i_L(s) = \frac{1}{1 + T_{vsi}(\mathrm{s})} i_{ref}(s) \tag{21}$$

Based on (19) and (21), as $T_{vsi}(\mathrm{s})$ approaches infinity, $i_L(\mathrm{s})$ approaches $i_{ref}(\mathrm{s})$ and $e(s)$ approaches zero. Because $i_{ref}(\mathrm{s})$ is sinusoid, it is required to make $T_{vsi}(\mathrm{s})$ infinite at the line frequency.



(a)



(b)

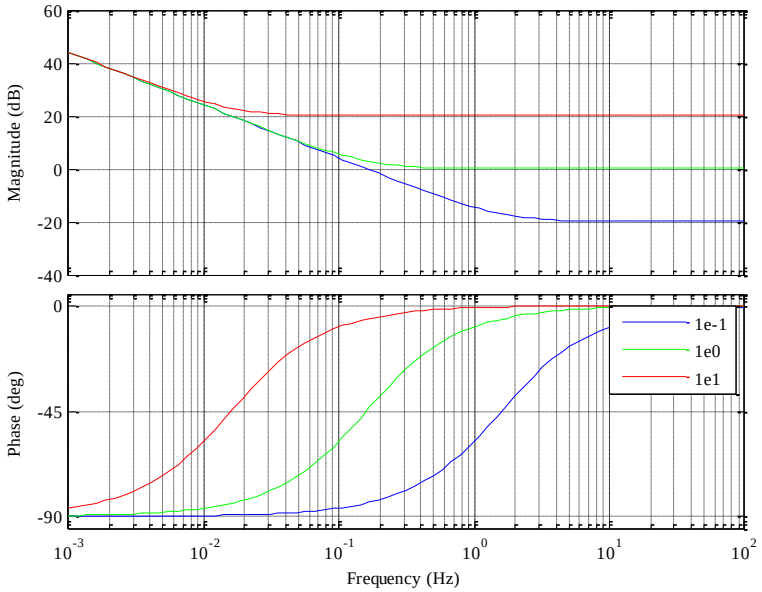
Fig. 10. Block diagram of the VSI (a) Without feed-forward (b) With feed-forward

3.1.1 PI Controller

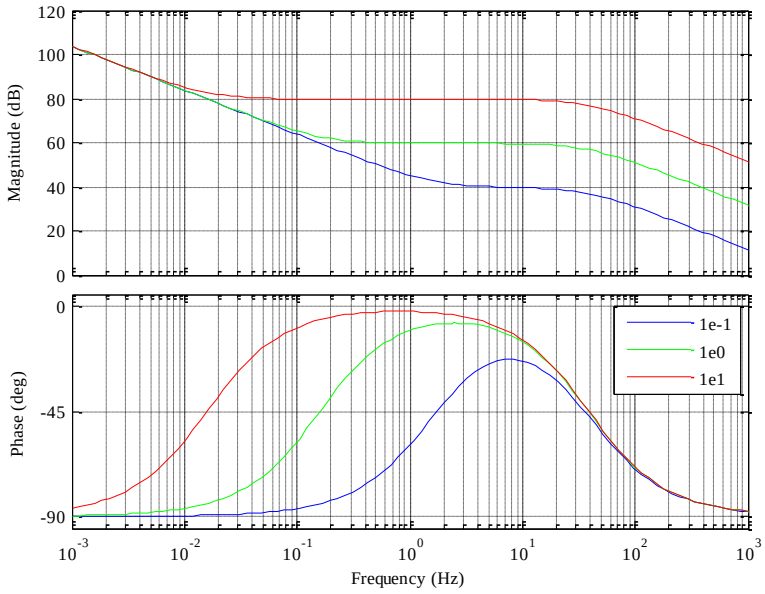
The PI controller is widely used in industrial field because its gains are easily adjusted by trial and error method. The PI controller is expressed as follows:

$$G_{PI}(s) = k_{pi} + \frac{k_{ii}}{s} \tag{22}$$

There are two parameters in the PI controller. A parameter k_{pi} is the proportional gain and k_{ii} is the integral gain. For simplicity of analysis, one of the two is assumed to be constant while the other affect the frequency responses. First, k_{ii} is assumed to be constant. As shown in Fig. 11(a), the magnitude responses of the PI controller increase at the high frequencies with increasing k_{pi}. Therefore, the magnitude responses of the current loop increase at the high frequency and the crossover frequency goes up as shown in Fig. 11(b).



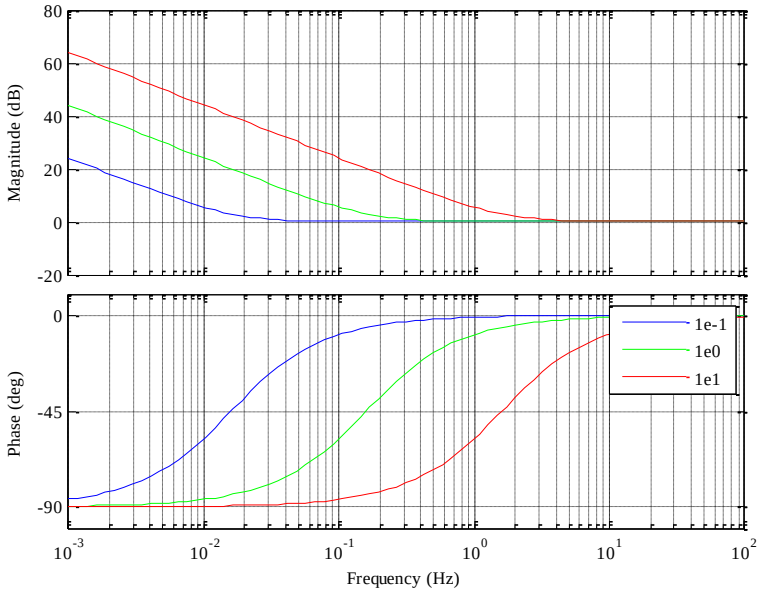
(a)



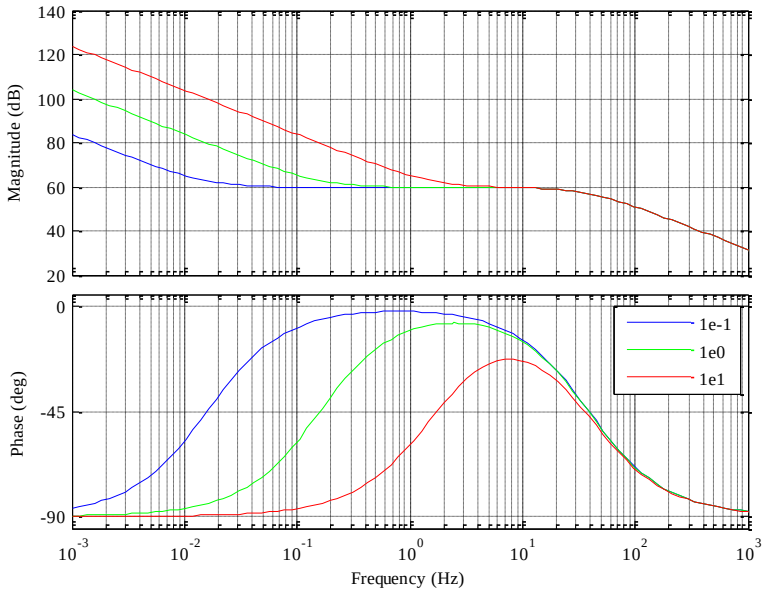
(b)

Fig. 11. Bode plots according to k_{pi} (a) Current controller (b) Current loop

Next, assuming that k_{pi} is the constant, as shown in Fig. 12(a), the magnitude responses of the PI controller increase at the low frequency with increasing k_{ii}. Therefore, the magnitude responses of the current loop increase at the low frequency as shown in Fig. 12(b).



(a)



(b)

Fig. 12. Bode plots according to k_{ii} (a) Current controller (b) Current loop

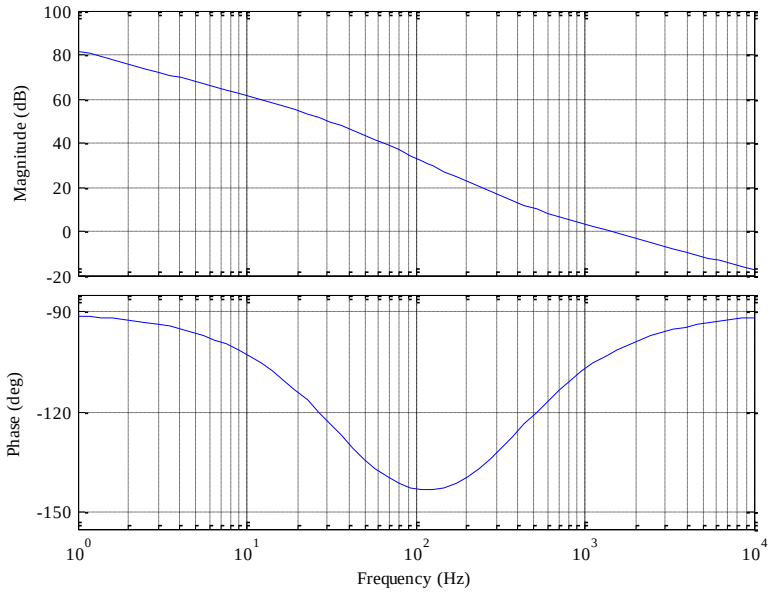
When the PI controller is adopted as the current controller, and the characteristic equation which is the denominator of (20) can be expressed as follows:

$$Ls^2 + (r_l + V_{dc}k_{pi})s + V_{dc}k_{ii} = 0 \tag{23}$$

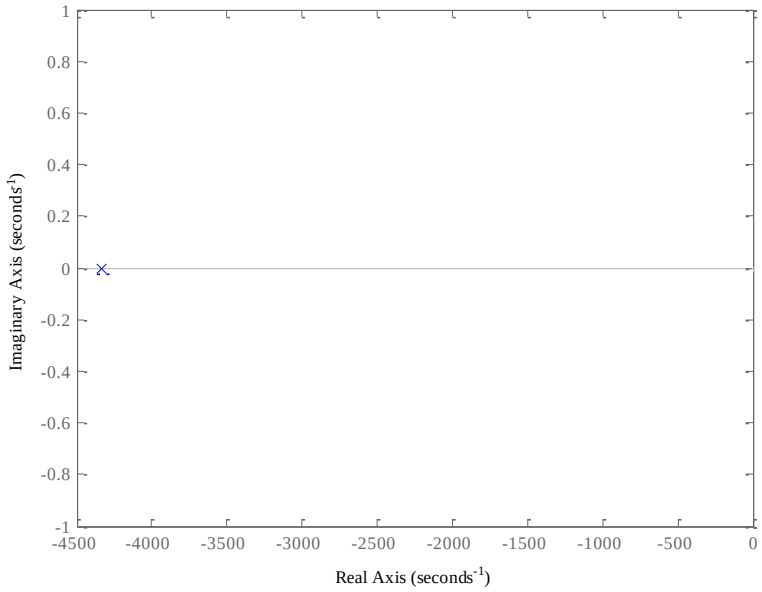
When the characteristic equation is quadratic polynomial, it has to have one real double root to obtain the fastest transient response without an overshoot. For a critical damping condition, the discriminant has to be equal to zero. Thus, k_{pi} and k_{ii} have the relationship as follows:

$$k_{pi} = f(k_{ii}) = -\frac{r_l + \sqrt{4LV_{dc}k_{ii}}}{V_{dc}} \tag{24}$$

The value of k_{pi} is chosen to limit the crossover frequency lower than the ten percent of the switching frequency. As shown in Fig. 13(a), the magnitude of the designed current loop at the line frequency is 40 dB and the crossover frequency is Hz. Fig. 13(b) shows that the system has one real double root.



(a)



(b)

Fig. 13. Designed current loop adopting the PI controller (a) Bode plot of the current loop (b) Pole map

The PI controller has an infinite gain at dc (0 Hz) so it is suitable to track the dc reference. However, it is not good for tracking the sinusoidal reference due to its finite gain at the line frequency. The lower crossover frequency induces the smaller current loop gain.

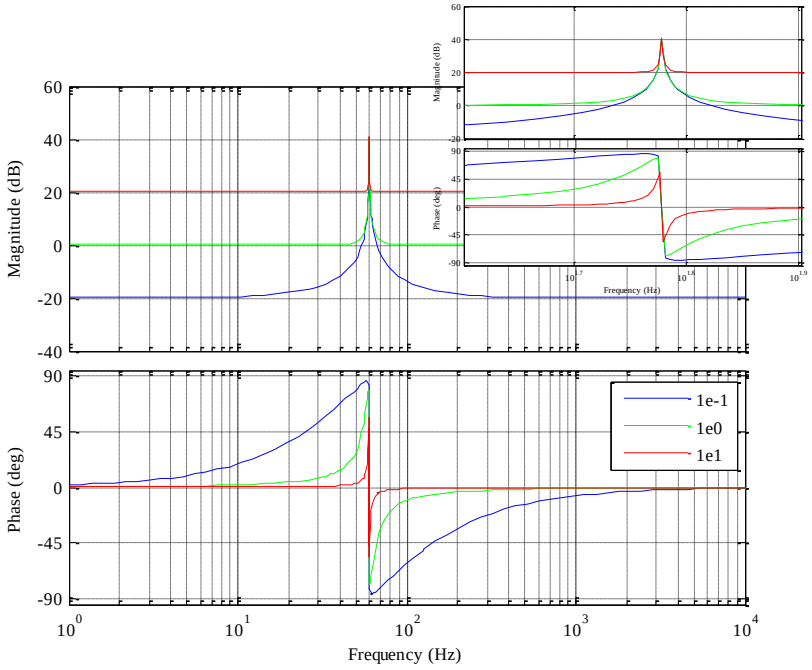
3.1.2 PR Controller

The PR controller which introduces the large gain at the specific frequency ω_0 can track the sinusoidal reference without the steady-state error. The expression of PR controller is as follows:

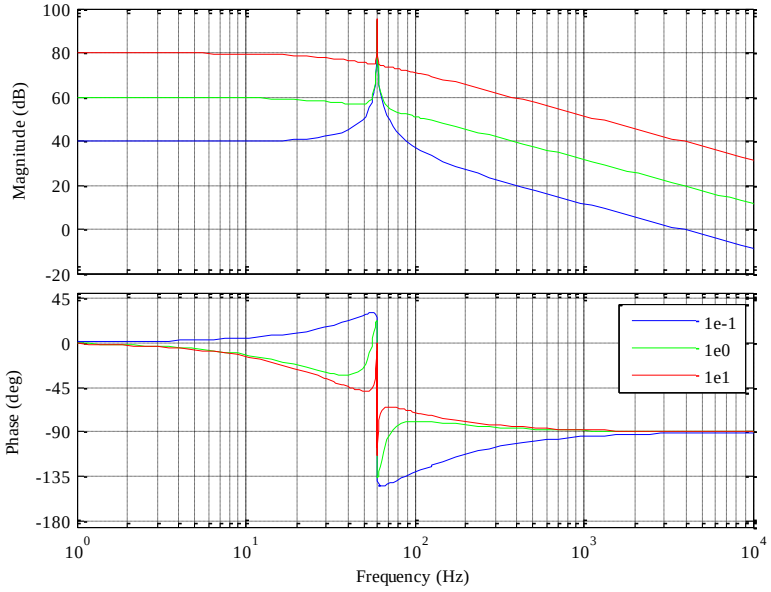
$$G_{PR}(s) = k_p + \frac{2k_r\xi\omega_0 s}{s^2 + 2\xi\omega_0 s + \omega_0^2} \tag{25}$$

Because it is desired that the current is synchronous with the grid voltage, ω_0 is assigned to the line frequency. Accordingly, there are three unassigned parameters in the PR controller. Firstly, k_r and ξ are assumed to be constant for simple analysis of the effect of k_p on the frequency responses. As shown in Fig. 14(a) and Fig. 14(b), with increasing k_p, the magnitude of the current controller and the

current loop increases for all frequencies except for ω_0. Therefore, the crossover frequency of the current loop is increased as k_p increases.



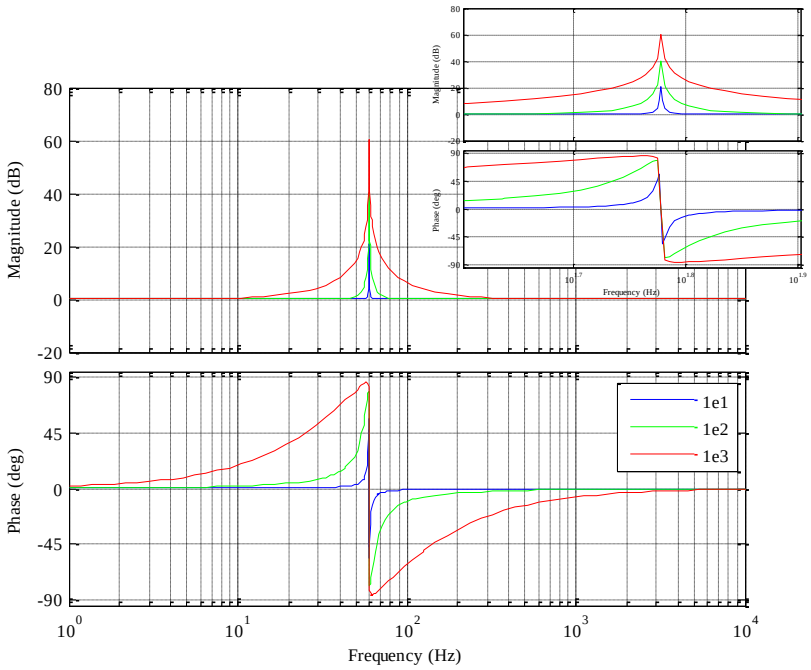
(a)



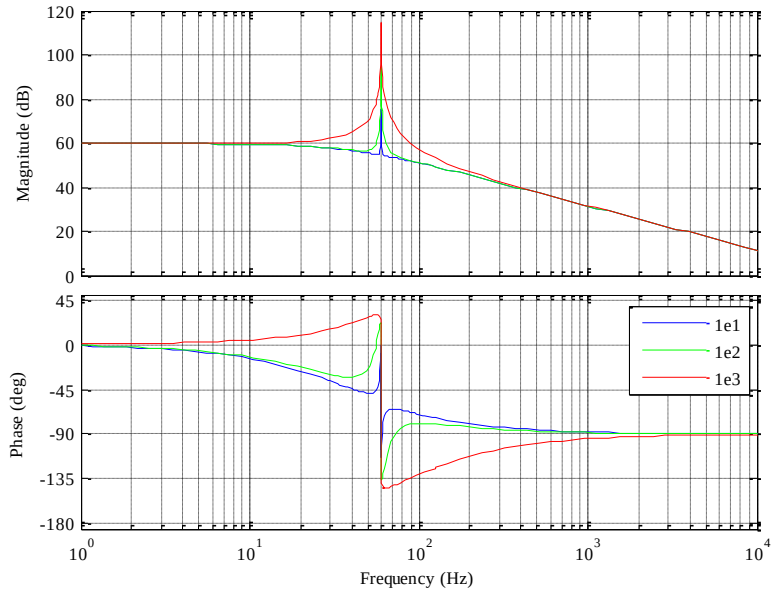
(b)

Fig. 14. Bode plots according to k_p (a) Current controller (b) Current loop

Secondly, k_p and ξ are assumed to be constant to analyze the effect of k_r on the frequency responses. Fig. 15(a) and Fig. 15(b) show the frequency responses of the current controller and the current loop, respectively. As k_r increases, the magnitude at ω_0 increases. If the crossover frequency of the current loop is far from the line frequency, k_r has no influence on the crossover frequency.



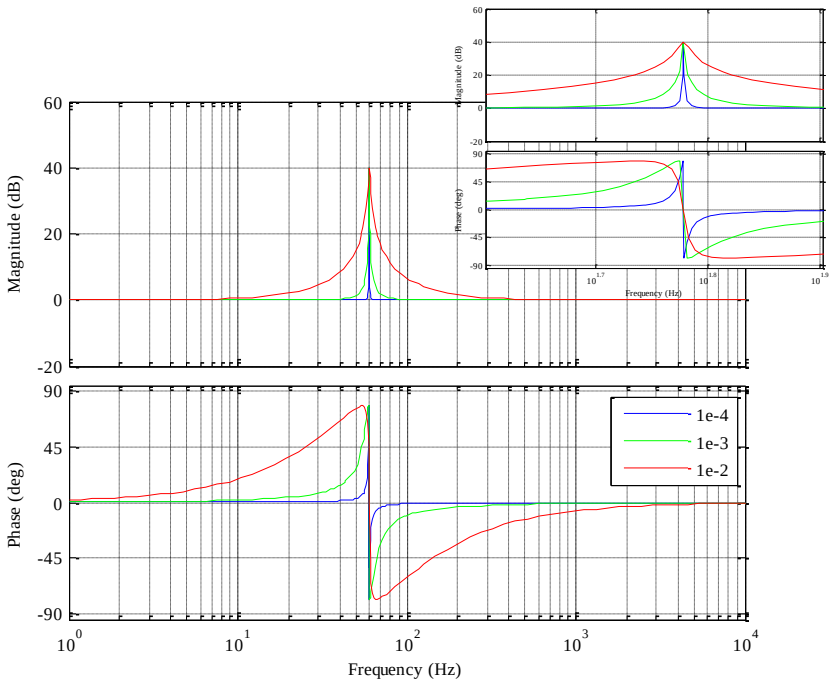
(a)



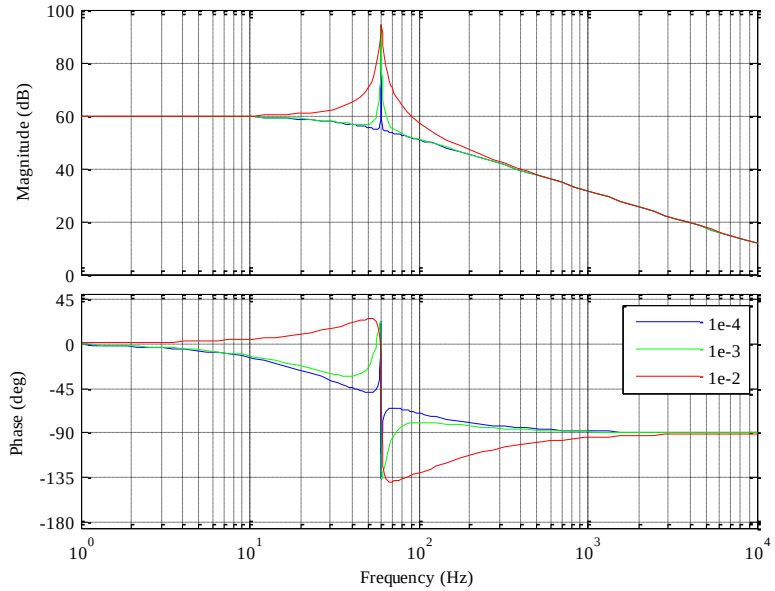
(b)

Fig. 15. Bode plots according to k_r (a) Current controller (b) Current loop

Finally, k_p and k_r are assumed to be constant to analyze the effect of ξ on the frequency responses. In Fig. 16(a) and Fig. 16(b), with increasing ξ, the magnitude near the resonant frequency increases. However the magnitude at ω_0 is fixed. In common with k_r, ξ does not influence the crossover frequency of the current loop if the crossover frequency is much higher than ω_0.



(a)



(b)

Fig. 16. Bode plots according to ξ (a) Current controller (b) Current loop

When the crossover frequency is the ten percent of the switching frequency, it is far higher than the resonant frequency and is determined only by k_p. The magnitude of the current loop at the line frequency is determined by k_r. After designing k_p and k_r, ξ sets the gain and the phase near the resonant frequency. In this thesis, the current loop gain of 60 dB at the resonant frequency is selected to achieve the ten times the loop gain adopting the PI controller. Fig. 17 shows the designed current loop.

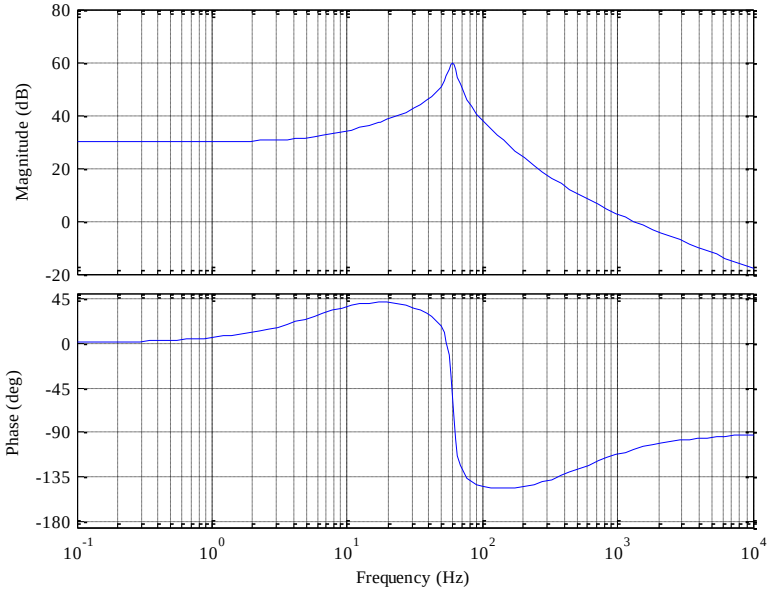


Fig. 17. Bode plot of the designed current loop adopting the PR controller

As mentioned earlier, the PR controller can have the enough gain at the line frequency regardless of the crossover frequency. Therefore, the steady-state error can be removed effectively. However, the PR controller has the error when the input is the step function. Based on the final value theorem, the steady-state error can be calculated in respect to the step input. Final value theorem is defined as

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} se(s) \tag{26}$$

where $e(t)$ is the steady-state error in time domain and $e(s)$ is Laplace transform of $e(t)$. Based on (21) and Fig. 10(b), the error can be expressed as follows:

$$e(s) = \frac{\frac{\omega_0}{(s^2+\omega_0^2)}}{1+T_{vsi}(s)} i_{mag}(s) \tag{27}$$

Thus, the steady-state error regarding the step input is calculated as follows:

$$\lim_{s\to 0} s \frac{\frac{\omega_0}{s(s^2+\omega_0^2)}}{1+T_{vsi}(s)} = \frac{r_l}{\omega_0(r_l+V_{dc})} \tag{28}$$

3.1.3 PIR Controller

Recently, the PIR controller has been studied for three-phase applications. The PIR controller has the advantage of regulating both ac and dc components. In this thesis, the PIR controller is proposed to enable both tracking the sinusoidal reference and removing the steady-state error generated by step input and step load variations for single-phase inverter applications. The PIR controller consists of the PI controller and the PR controller. The expression of the PIR controller is as follows.

$$G_{PIR}(s) = k_p + \frac{k_i}{s} + \frac{2k_r\xi\omega_0 s}{s^2+2\xi\omega_0 s+\omega_0^2} \tag{29}$$

Fig. 18 shows the difference of frequency response between the conventional PR controller and the proposed PIR controller. The proposed PIR controller has large gain at the line frequency, which is similar to the conventional PR controller. In addition, by helping from the integrator, it has an infinite gain at dc. Based on the final value theorem, the PIR controller has no steady-state error.

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} se(s) = \lim_{s\to 0} s \frac{\frac{\omega_0}{s(s^2+\omega_0^2)}}{1+T_{vsi}(s)} = 0 \tag{30}$$

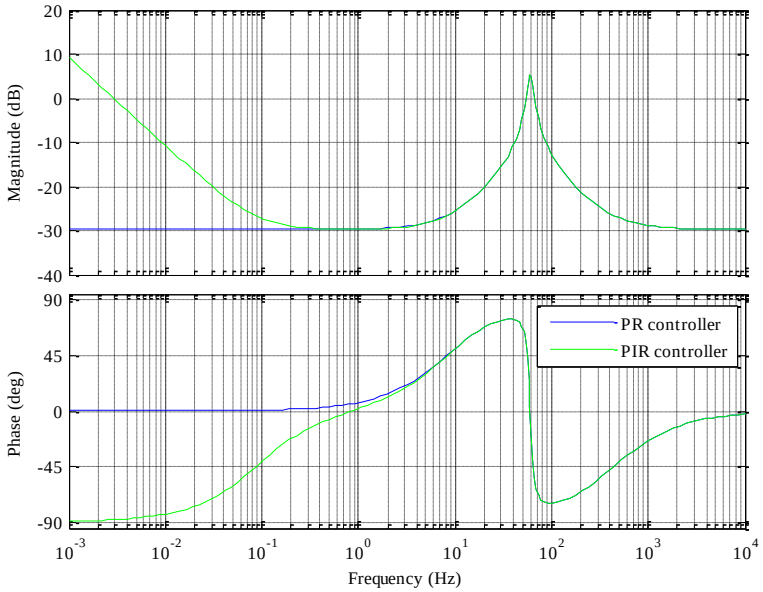
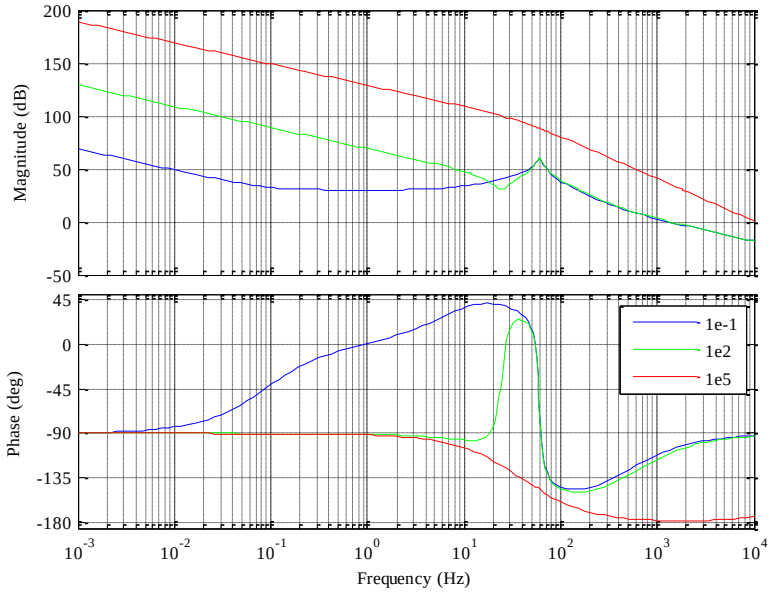
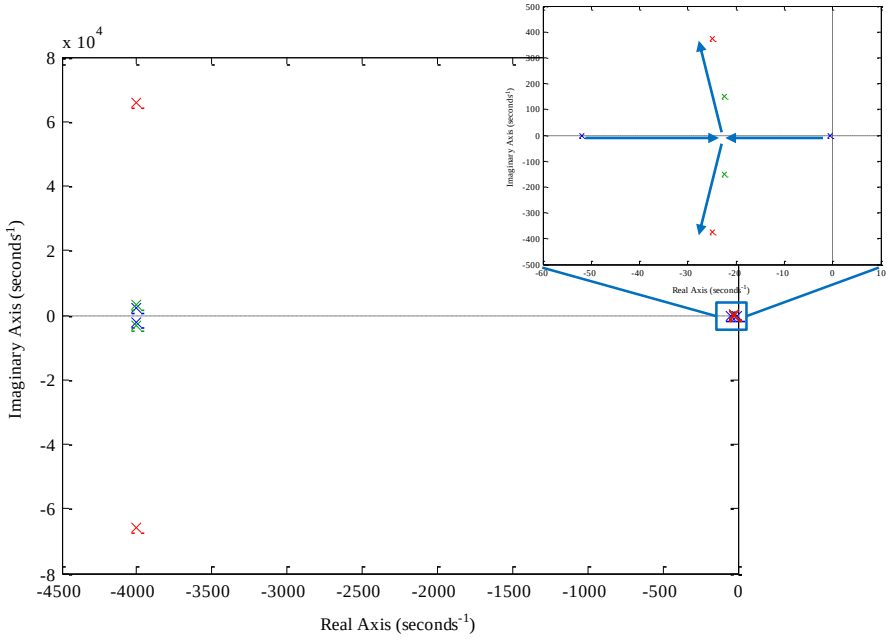


Fig. 18. Frequency responses of the PR controller and the PIR controller

In order to design the PIR controller, the effect of the integral gain k_i should be considered. In Fig. 19 (a), as k_i increases, the magnitude responses of the proposed controller is similar to a single integrator and the phase margin decreases. Fig. 19 (b) shows the movement of poles with respect to k_i. Arrows indicate the directions according to increasing k_i. It shows that the peaking of the magnitude increases with increasing k_i by dominant poles. Therefore, the value of k_i which places the dominant poles at the breakaway point is selected to obtain the fastest transient response without the magnitude peaking.



(a)



(b)

Fig. 19. Effects of k_i (a) Bode plot of the current loop (b) Pole map

Fig. 20 shows the frequency responses of the designed current loop adopting the PIR controller. It has the same crossover frequency and phase margin with the PR controller.

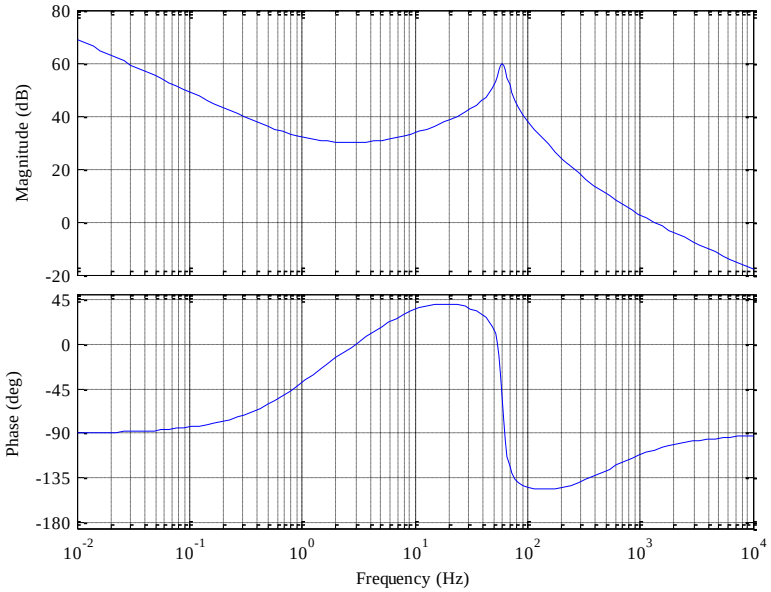
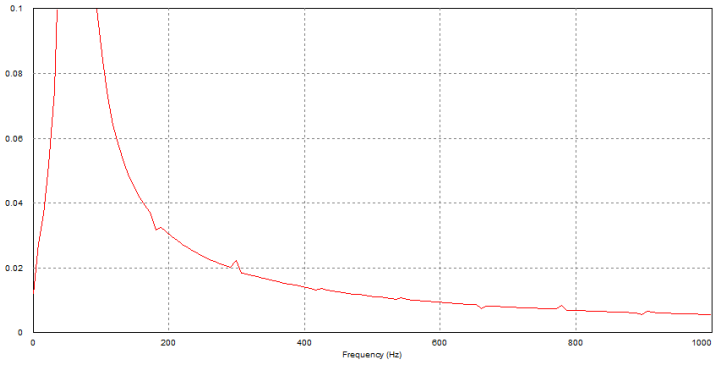


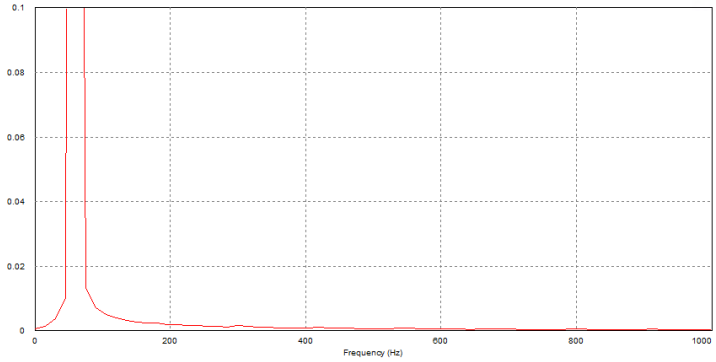
Fig. 20. Bode plot of the designed current loop adopting the PIR controller

3.1.4 Simulation Results

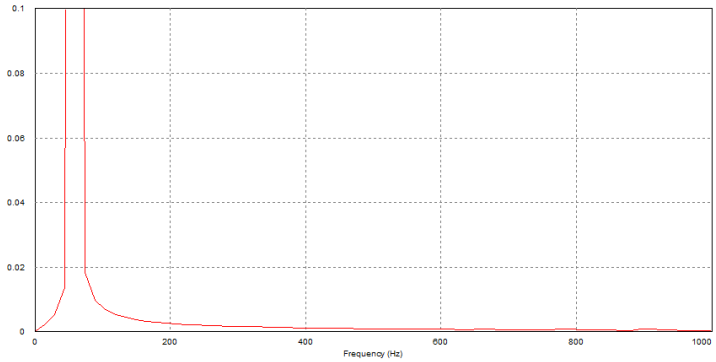
The PIR controller is verified by PSIM simulation. In Fig. 21, normalized fast Fourier transform (FFT) results shows the frequency contents of the inductor current. The PR controller and the PIR controller has better attenuation capacity than the PI controller.



(a)



(b)



(c)

Fig. 21. Normalized FFT results of the inductor current (a) PI controller (b) PR controller (c) PIR controller

Fig. 22 shows the steady-state error of controllers when input is the step function. The PI controller has the shortest settling time without steady-state error. The PR controller has the steady-state error. Even if the PIR controller is slower than the PI controller, its steady-state error converges to zero. In conclusion, in terms of the transient response speed and the steady-state error, the PIR controller has intermediate characteristics between the PI controller and the PR controller.

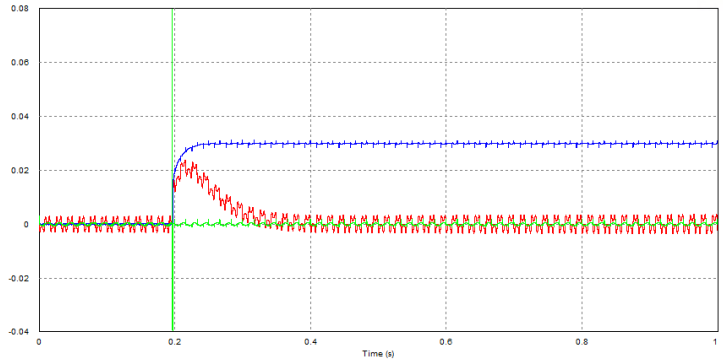


Fig. 22. Steady-state error generated by the step input (green : PI controller, blue : PR controller, red : PIR controller)

3.2 Voltage Controller Design

In this part, design of the voltage controller is investigated considering the audio-susceptibility and the output impedance, as well as the stability. Fig. 23 shows the small-signal block diagram of the variable dc link inverter. $G_{LPF}(s)$ represents the low pass filter and $G_{cv}(s)$ represents the voltage controller which determines the current reference. As shown in Fig. 24, there are two loops including the current loop $T_i(s)$ and the voltage loop $T_v(s)$. The expressions of loops are as follows:

$$T_i(s) = G_{ci}(s)G_{id}(s) \tag{31}$$

$$T_v(s) = -G_{ci}(s)G_{vd}(s)G_{LPF}(s)G_{cv}(s) \tag{32}$$

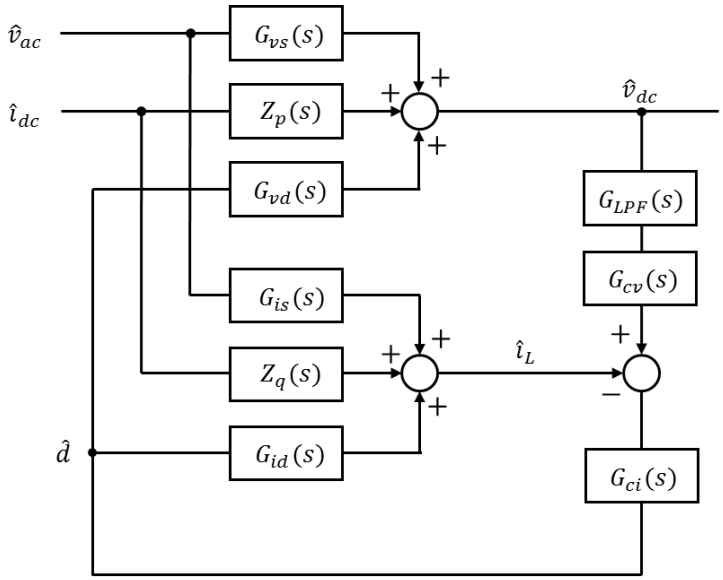
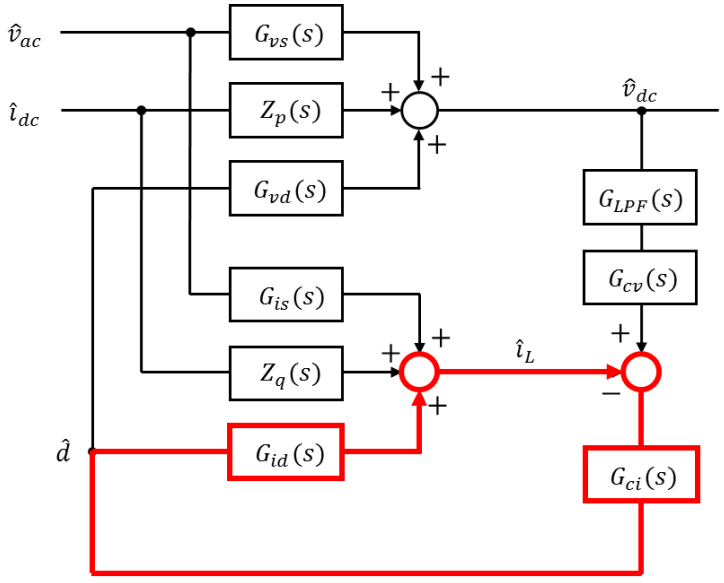
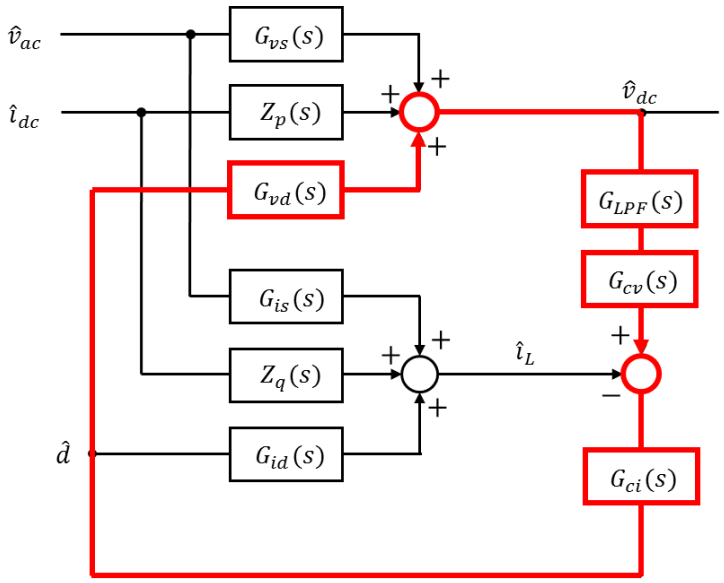


Fig. 23. Small-signal block diagram of the inverter



(a)



(b)

Fig. 24. Loops included in inverter system (a) Current loop (b) Voltage loop

The stability of the system including loops can be determined by the loop gain. An overall loop gain and an outer loop gain can be expressed as follows:

$$T_1(s) = T_i(s) + T_v(s) \tag{33}$$

$$T_2(s) = \frac{T_v(s)}{1 + T_i(s)} \tag{34}$$

As the performance criteria, the audio-susceptibility and the output impedance are defined. The audio-susceptibility describes the noise transmission characteristics from the grid voltage to the dc link voltage and can be expressed as (35). The output impedance describes the noise transmission characteristics from the dc side current to the dc link voltage and can be expressed as (36). For the constant dc link voltage, both should be minimized. From (35) and (36), the audio-susceptibility and the output impedance are affected by the overall loop gain.

$$A_u(s) = \frac{\hat{v}_{dc}(s)}{\hat{v}_{ac}(s)}\Big|_{closed} = \frac{G_{vs}(s)(1+T_i(s)) - G_{is}(s)G_{ci}(s)G_{vd}(s)}{1+T_1(s)} \tag{35}$$

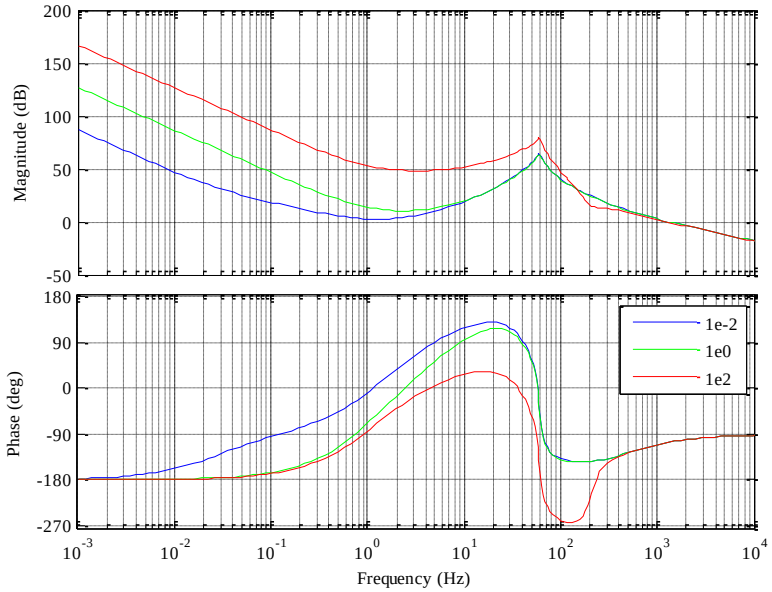
$$Z_o(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}_{dc}(s)}\Big|_{closed} = \frac{Z_p(s)(1+T_i(s)) - Z_q(s)G_{ci}(s)G_{vd}(s)}{1+T_1(s)} \tag{36}$$

Because the reference value of the voltage controller is constant, the PI controller is adopted to control the dc link voltage. The PI controller is effective to track the dc reference due to its infinite gain at dc. The expression of the voltage controller is as follows:

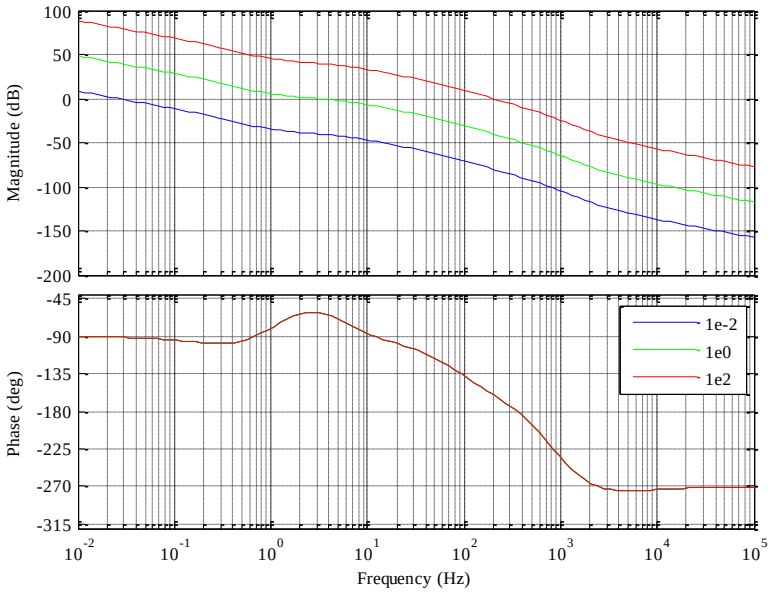
$$G_{PIv}(s) = k_{pv} + \frac{k_{iv}}{s} = k_{iv}\frac{1+\frac{s}{\omega_{zv}}}{s} \tag{37}$$

There are two parameters to design. In the same manner as that current controller design, one of the two is assumed to be constant while the other affect the frequency responses. First, it is assumed that ω_{zv} is the constant. As shown in Fig. 25(a), as k_{iv} increases, the overall loop gain increases at the low frequency. Thus, the audio-susceptibility and the output impedance characteristics are improved at the low frequency. In Fig. 25(c) and Fig. 25(d), dashed lines represent the open loop characteristics.

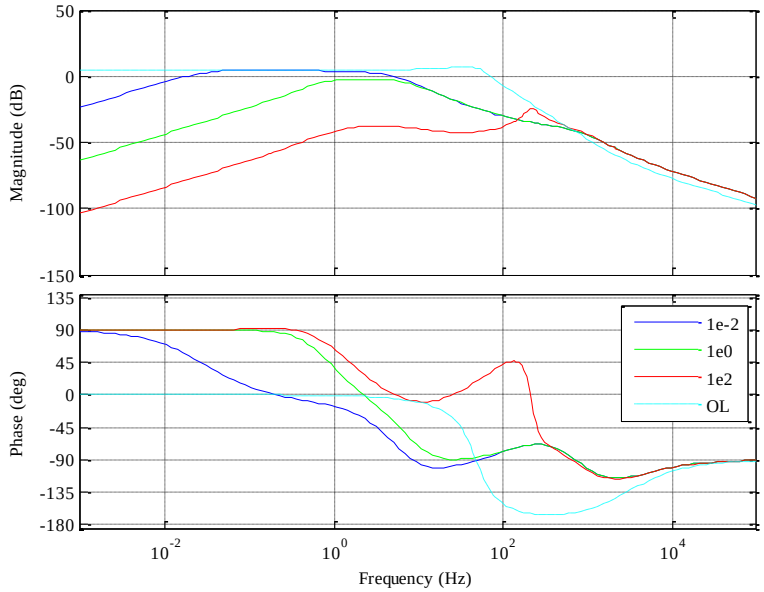
The overall loop gain and the outer loop gain give the same absolute stability information but different relative stability information. The overall loop gain that is defined as the sum of the voltage loop and the current loop has extra gain margin and phase margin. Also, the outer loop gain gives the stability information of the voltage loop when the current loop is prefixed. Therefore, the outer loop gain is judged as being more informative [19]. Fig. 25(b) shows the frequency responses of the outer loop gain. As k_{iv} increases, magnitude response graphs go up, maintaining its shape. Meanwhile, the frequency responses have no relation to k_{iv}.



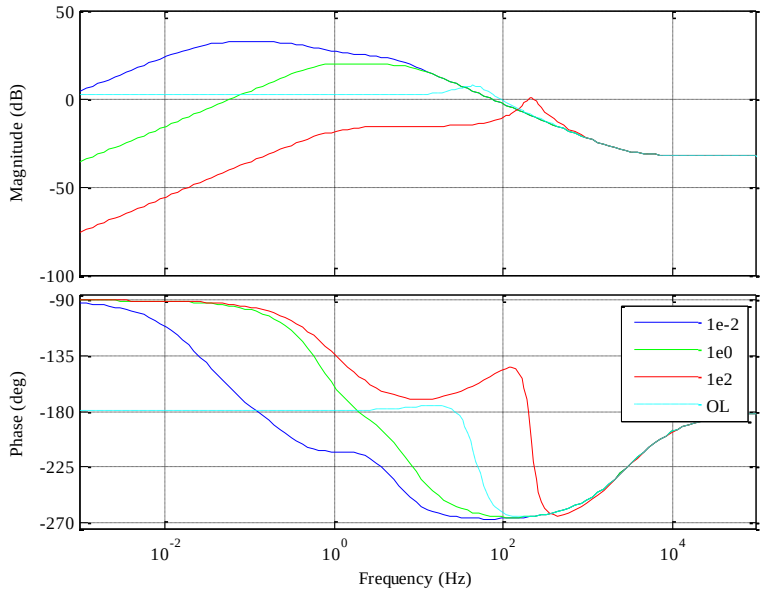
(a)



(b)



(c)

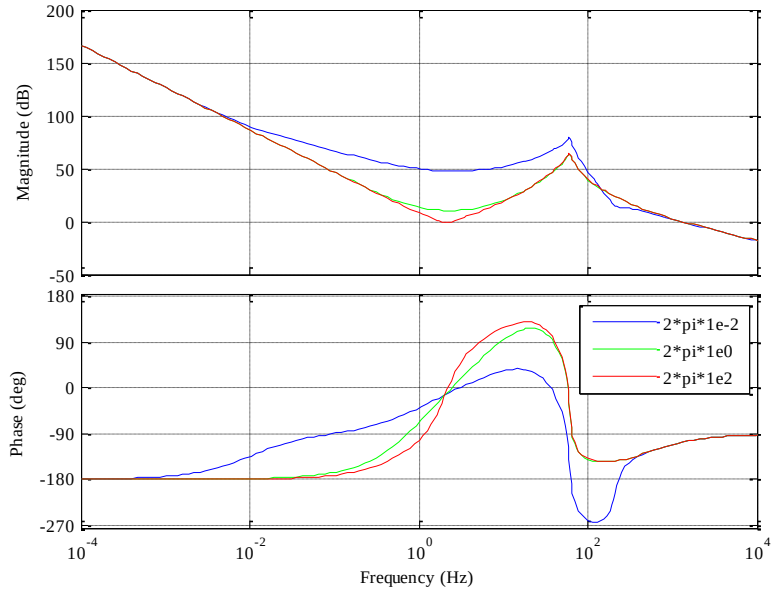


(d)

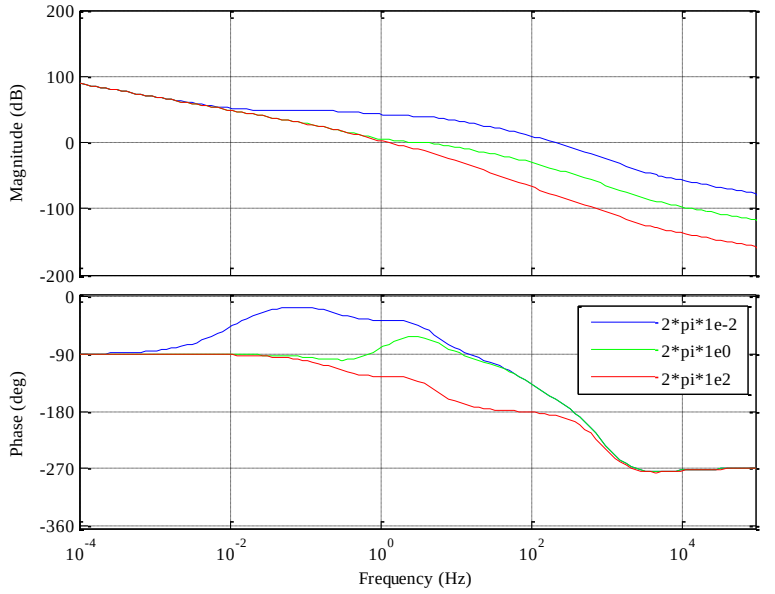
Fig. 25. Bode plots according to k_{iv} (a) Overall loop gain (b) Outer loop gain (c) Audio-susceptibility (d) Output impedance

Second, k_{iv} is assumed as the constant. In Fig. 26(a), as ω_{zv} increases, the overall loop gain decreases in some frequency range. Therefore, the audio-susceptibility and the output impedance

deteriorate in that range of frequency as shown in Fig. 26(c) and Fig. 26(d). In Fig. 26(b), the high frequency gain decreases and the crossover frequency moves to the left with increasing ω_{zv}.



(a)



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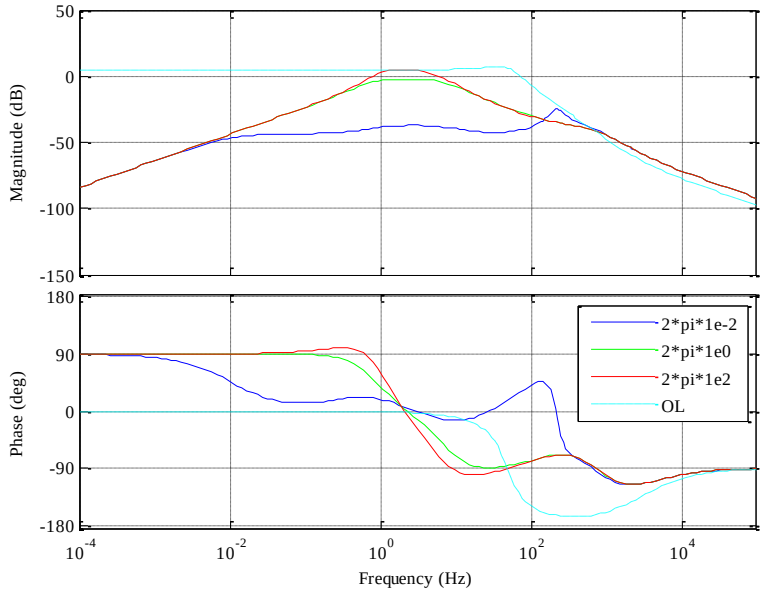
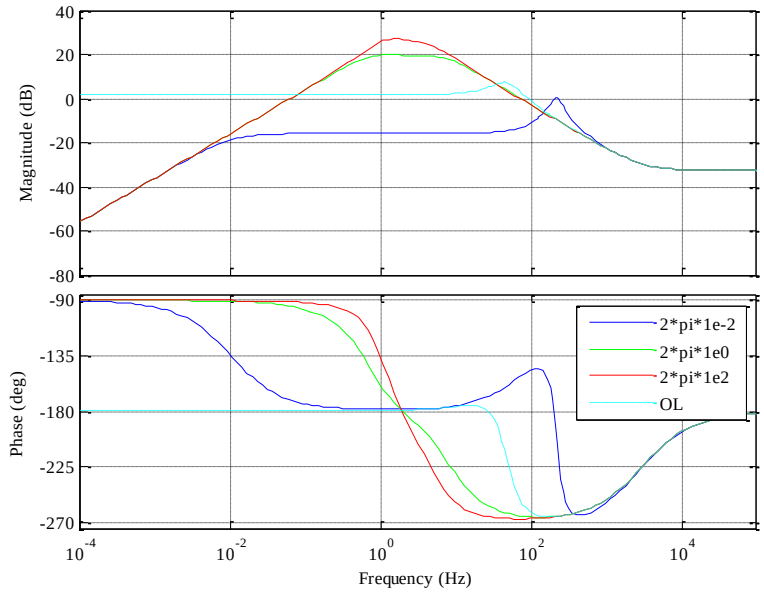


(c)



(d)

Fig. 26. Bode plots according to ω_{zv} (a) Overall loop gain (b) Outer loop gain (c) Audio-susceptibility (d) Output impedance

For the purpose of obtaining proper dynamics and stability, the crossover frequency and the phase margin are considered. Because there are double line frequency ripples in the dc link voltage, the crossover frequency of the outer loop gain is limited to twenty percent of the line frequency. Because

k_{iv} has no impact on the phase response, the phase margin is adjusted by varying ω_{zv}. On the other hand, the crossover frequency is affected by both k_{iv} and ω_{zv}. Thus, the crossover frequency is designed after ω_{zv} is prefixed. Fig. 27 shows the frequency responses of the designed outer loop gain under various load conditions. The stability of the system should be guaranteed within the operating range. Table 2 shows that the phase margins are maintained around 60 ˚ while the crossover frequencies are kept around 12 Hz for three load conditions.

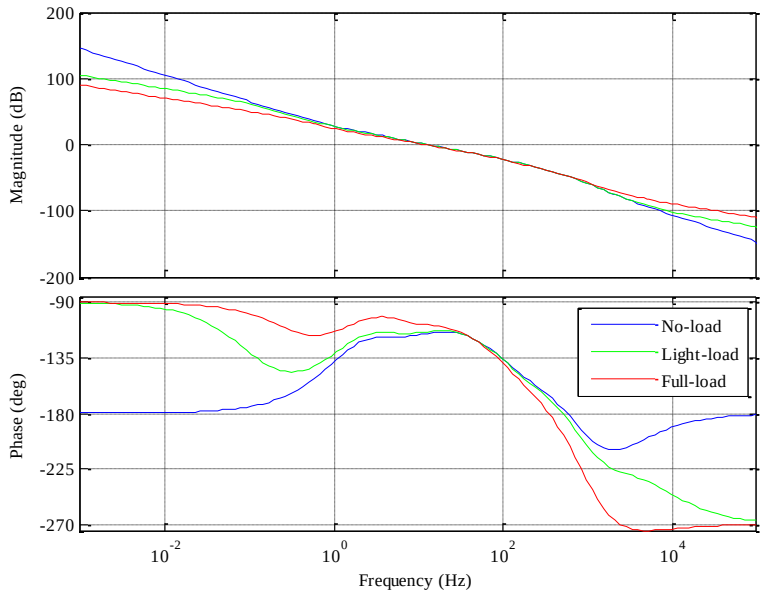


Fig. 27. Bode plots of the outer loop under various load conditions

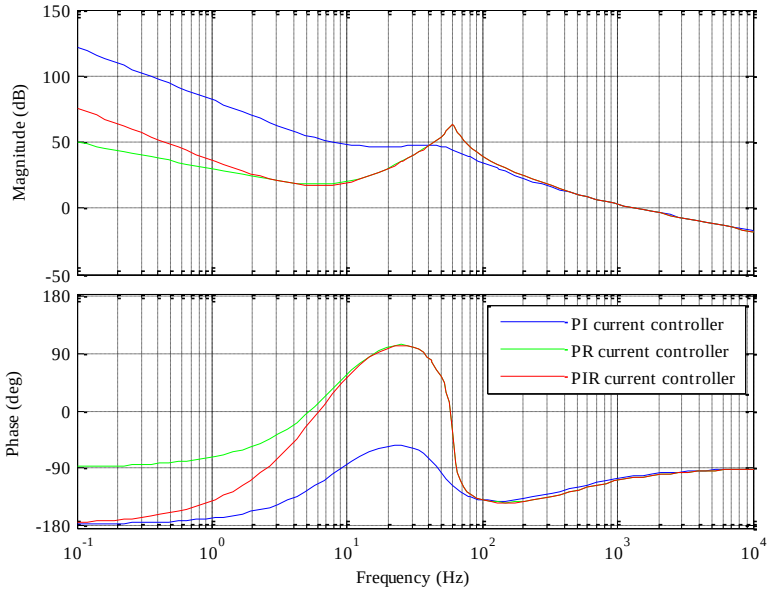
TABLE II

STABILITY INFORMATION UNDER VARIOUS LOAD CONDITIONS

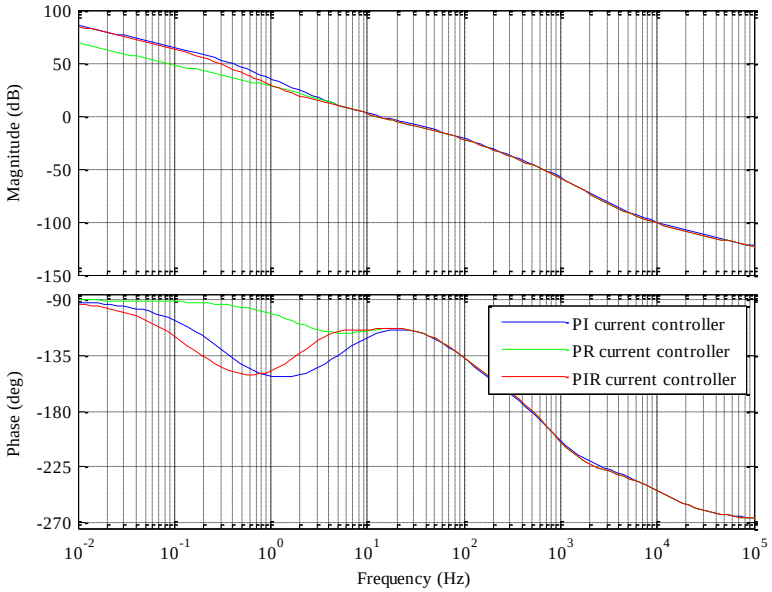
Load condition	No-load	Light-load	Full-load
Gain margin	50.1 dB	48 dB	41.5 dB
Phase margin	63.6 ˚	65 ˚	70.8 ˚
Crossover frequency	12.3 Hz	12.2 Hz	11.6 Hz

In the same way, the PI voltage controller is designed for the cases that the PI controller and the PR controller are used as the current controller. Fig. 28 shows the frequency responses of three kinds of current controllers. As shown in Fig. 28(b), when the PI controller and the PR controller are used for current control, outer loop gains are designed for the same crossover frequency and phase margin as the

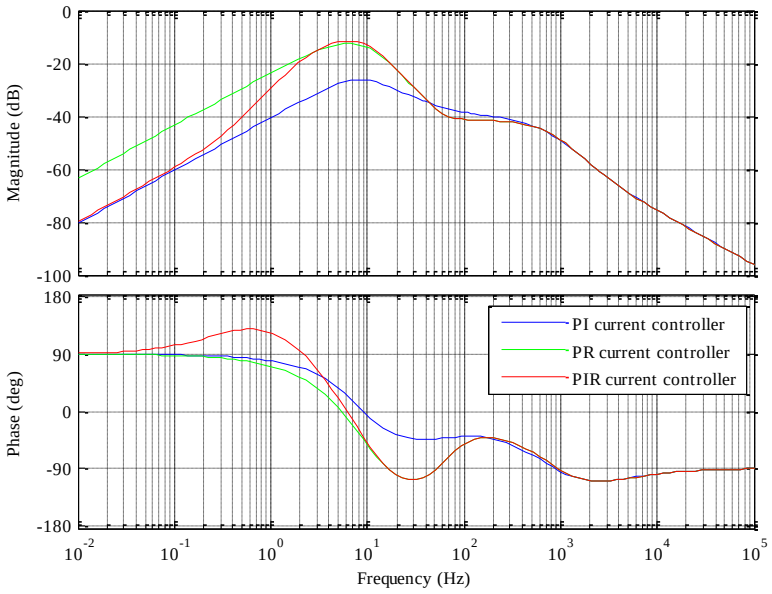
PIR current controller. In Fig. 28(a), at the low frequency, the overall loop gain has the largest magnitude when the PI controller is adopted to control the current. On the other hand, at the line frequency, the PR current controller and the PIR current controller have larger gain compared to the PI current controller. Therefore, the audio-susceptibility is the lowest at the low frequency when the PI current controller is used and is the lowest at the line frequency when the PR current controller and the PIR current controller are used. The PIR current controller has better attenuation capability than the PR controller at the low frequency and than the PI controller at the line frequency for variations in the grid voltage. Three output impedance lines are similar each other for all frequencies. Thus, similar responses of the dc link voltage are expected at the presence of variations in the dc side current for three current controllers.



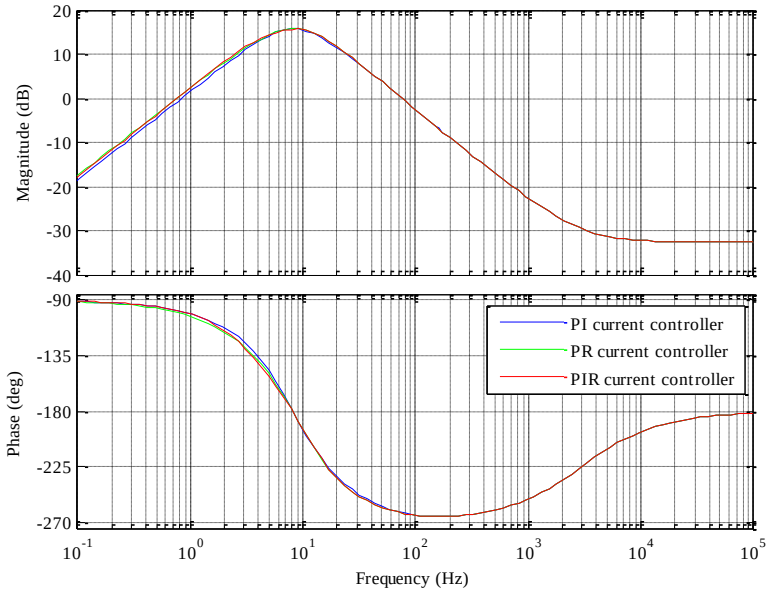
(a)



(b)



(c)



(d)

Fig. 28. Bode plots with three kinds of current controllers (a) Overall loop gain (b) Outer loop gain (c) Audio-susceptibility (d) Output impedance

Transient behavior of the dc link voltage is investigated using step load response. Time-domain expression of the dc link voltage has the relationship to the output impedance as follows

$$\hat{v}_{dc}(t) = \mathcal{L}^{-1}\left\{\frac{I_{step}}{s} Z_o(s)\right\} \tag{38}$$

where $\mathcal{L}^{-1}$ is the inverse Laplace transformation and I_{step} is the magnitude of the step change in the dc side current [19]. Based on the asymptotic analysis method, the output impedance in Fig. 28(d) can be approximated as follows:

$$Z_o(s) = k_o \frac{s\left(1 + \frac{s}{\omega_z}\right)}{1 + \frac{s}{Q\omega_p} + \frac{s^2}{\omega_p^2}} \tag{39}$$

Fig. 29 shows the output impedance comparison. The solid line shows the exact equation of the output impedance and the dashed line shows the asymptotic approximation. The dashed line matches with the exact output impedance equation for all frequencies.

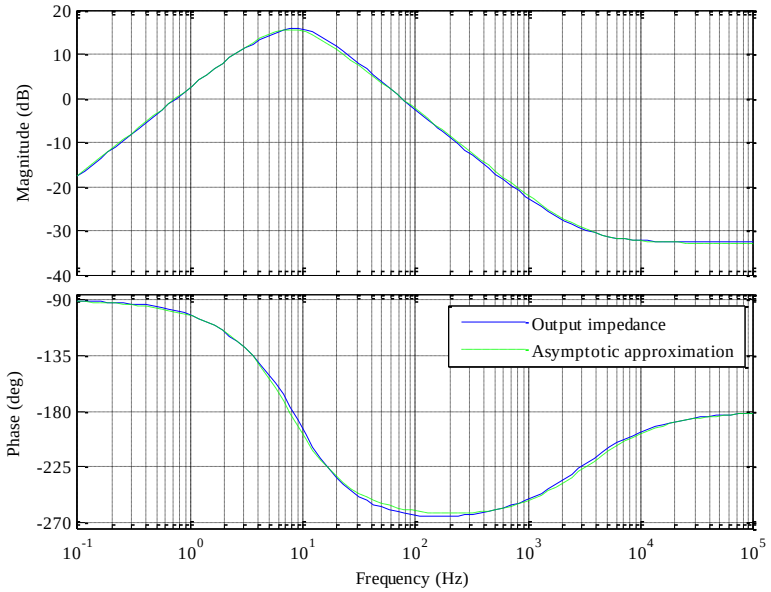


Fig. 29. Bode plot of the asymptotic approximation

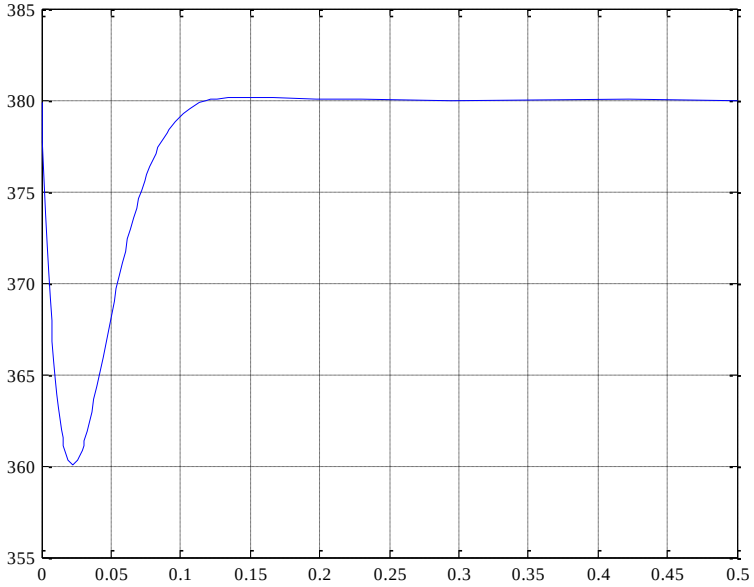
Using the asymptotic approximation, the time-domain dc link voltage can be expressed as

$$\hat{v}_{dc}(t) = \frac{I_{step} k_o \omega_p^2}{\omega_z} e^{-\frac{\omega_p}{2Q}t} \left(\cos At - \frac{\omega_z - \frac{\omega_p}{2Q}}{A} \sin At \right) \tag{40}$$

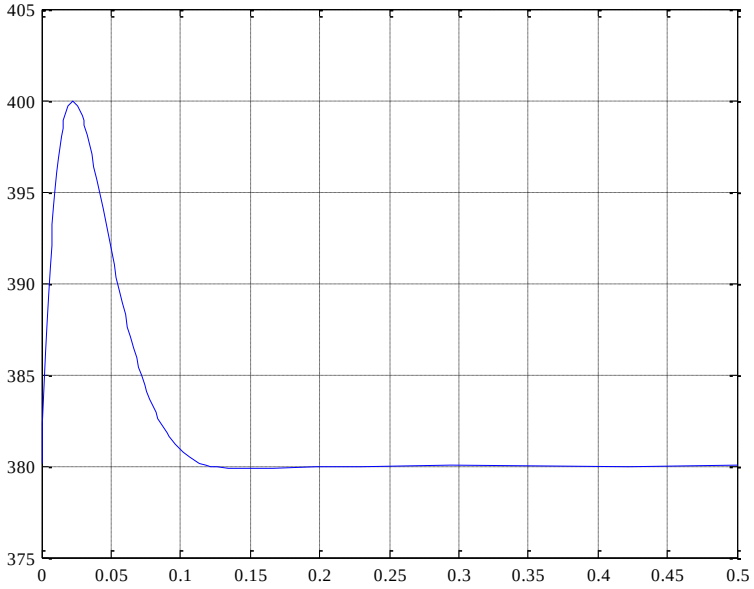
where

$$A = \frac{\omega_p \sqrt{Q^2 - \frac{1}{4}}}{\mathrm{Q}} \tag{41}$$

When the dc side current changes from 20 % to 70 % of full-load and vice versa, the absolute value of I_{step} is 4.34 A. In Fig. 30, the undershoot of 20 V and the overshoot of 20 V are expected for the dc link voltage from the asymptotic approximation. The expected settling time with 2 % tolerances above and below is 62 ms.



(a)



(b)

Fig. 30. Estimated dc link voltage with the step change in the dc side current (a) 20 % to 70 % load (b) 70 % to 20 % load

IV. EXPERIMENTAL RESULTS

The proposed small-signal model and controllers are verified by experiments. Circuit parameters used in experiments are listed in table 1. Fig. 31 shows the 3.3 kW single-phase grid-connected inverter prototype. The control strategy is implemented on the TI digital signal processor (DSP) TMS320F28335. The sampling frequency is set to be equal to the switching frequency of 13.8 kHz.

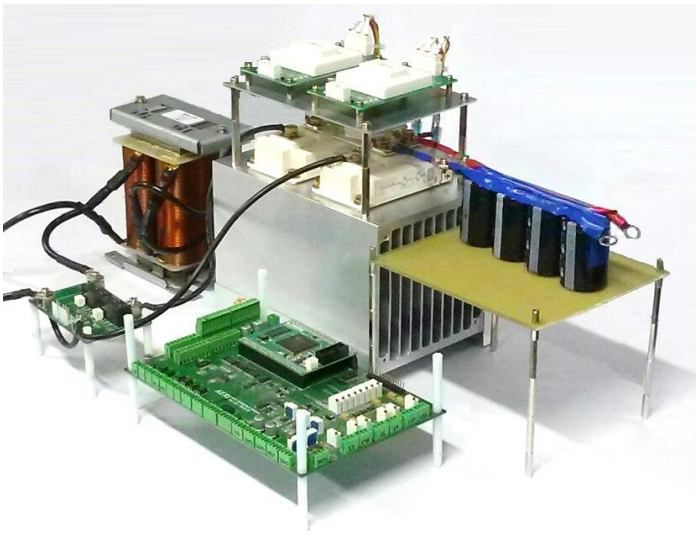
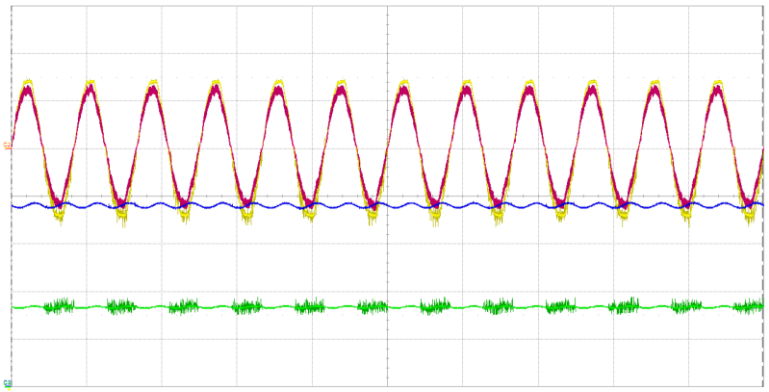


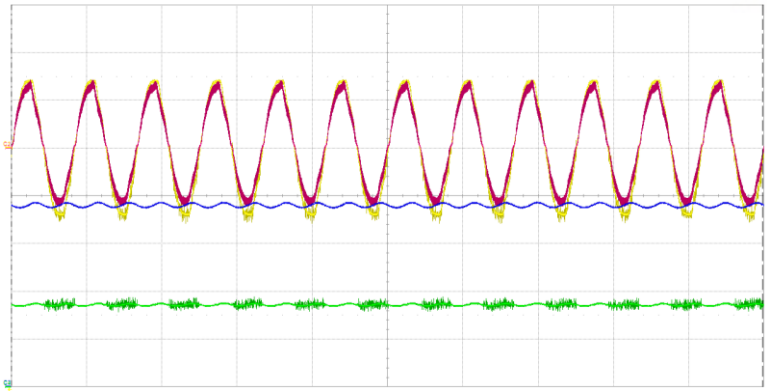
Fig. 31. Prototype of the 3.3 kW single-phase grid-connected inverter

Fig. 32 shows the steady-state waveform under the full-load condition with three kinds of current controllers. They have the PI voltage controller in common. When the PI controller, the PR controller and the PIR controller is adopted to control the current, magnitude of dc link voltage ripples are 14.1 V, 14.2 V and 14.4 V, respectively.



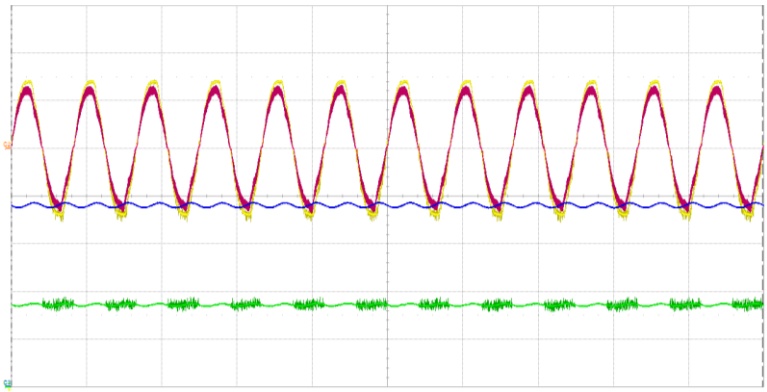
Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 20 ms/div

(a)



Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 20 ms/div

(b)

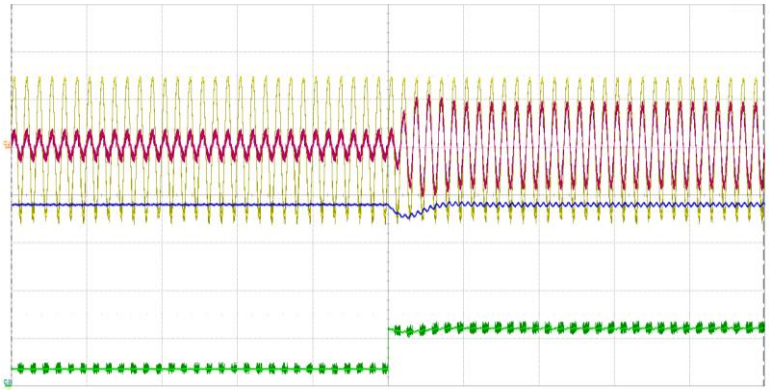


Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 20 ms/div

(c)

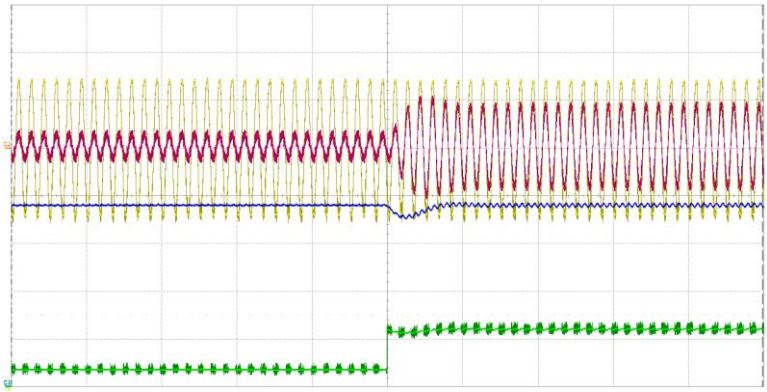
Fig. 32. Experimental results under the steady-state condition (a) PI current controller (b) PR current controller (c) PIR current controller

Fig. 33 and Fig. 34 show the corresponding experimental results to Fig. 30. Fig. 33 shows the undershoot waveforms that is occurred when dc side current changes from 20 % to 70 % load and Fig. 34 shows the overshoot waveforms that is occurred when dc side current changes from 70 % to 20 % load. Table 3 and table 4 show the difference between the expected value and the actual value of the undershoot, the overshoot and settling time. Because output impedances are the same regardless of the current controller, similar responses appear for the dc link voltage as expected. Allowing for that asymptotic approximation is used and ideal step load cannot be implemented in actual experimental condition, the error result from the small-signal model is negligible.



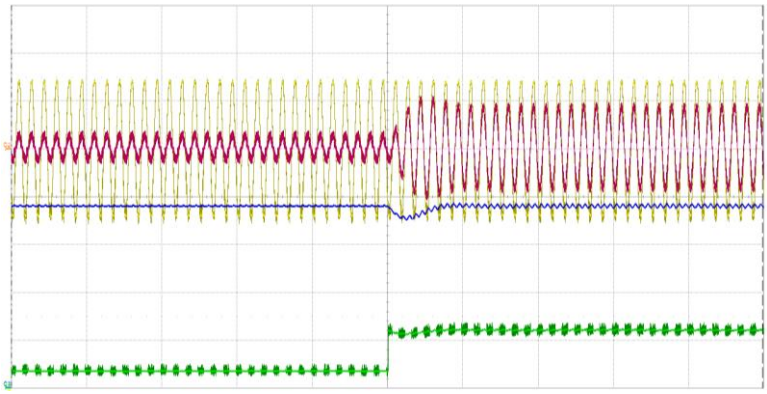
Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div

(a)



Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div

(b)



Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div

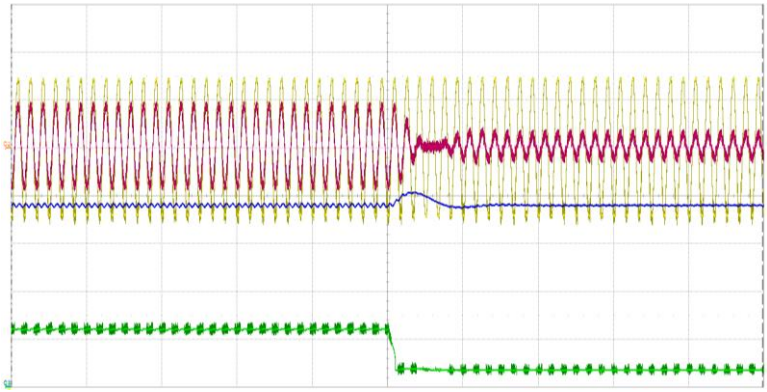
(c)

Fig. 33. Experimental results of step load response from 20 % to 70 % load (a) PI current controller (b) PR current controller (c) PIR current controller

TABLE III

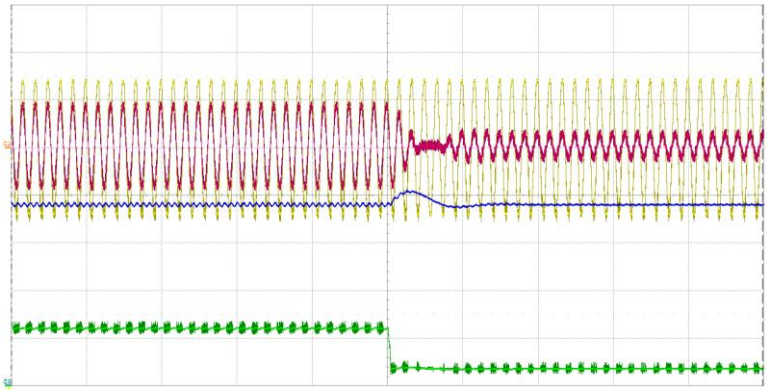
STEP LOAD RESPONSE ANALYSIS I

	Undershoot			Settling time		
	Expected	Actual	Error	Expected	Actual	Error
PI	5.26 %	5.28 %	0.25 %	62 ms	59.4 ms	4.19 %
PR	5.26 %	5.21 %	1 %	62 ms	59.42 ms	4.16 %
PIR	5.26 %	5.13 %	2.5 %	62 ms	59.2 ms	4.52 %



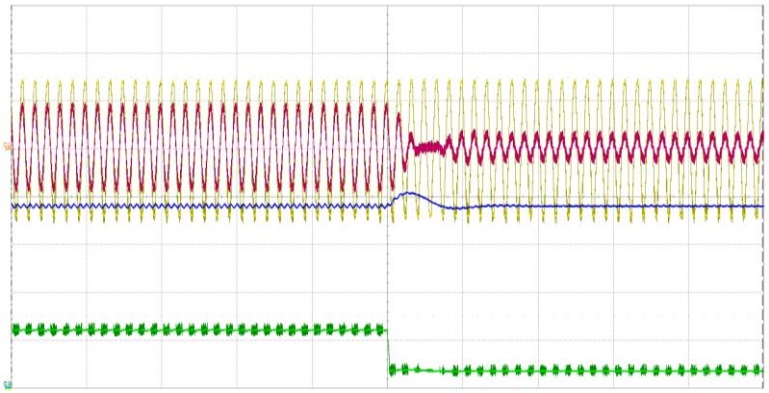
Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div

(a)



Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div

(b)



Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div

(c)

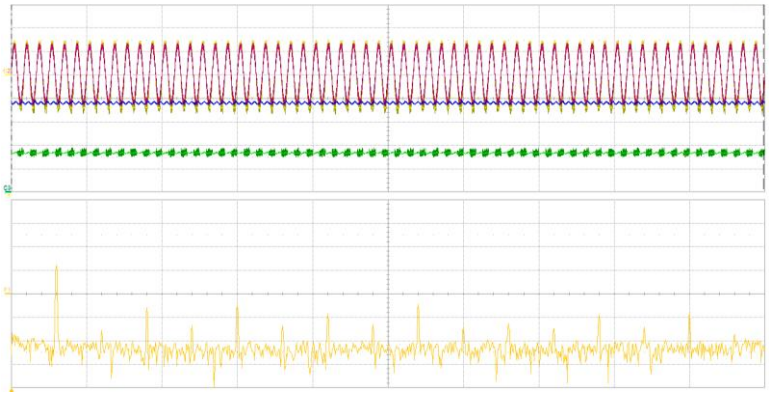
Fig. 34. Experimental results of step load response from 70 % to 20 % load (a) PI current controller (b) PR current controller (c) PIR current controller

TABLE IV

STEP LOAD RESPONSE ANALYSIS II

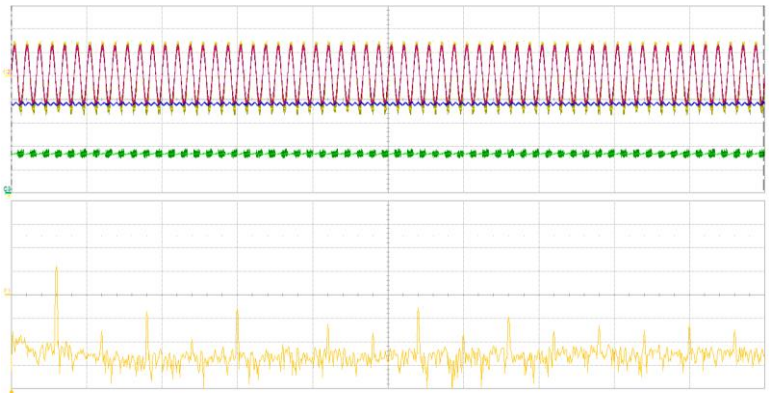
	Overshoot			Settling time		
	Expected	Actual	Error	Expected	Actual	Error
PI	5.26 %	5.12 %	2.75 %	62 ms	60.04 ms	3.16 %
PR	5.26 %	5.53 %	5 %	62 ms	60.14 ms	3 %
PIR	5.26 %	5.66 %	7.5 %	62 ms	60.14 ms	3 %

The harmonic suppression capability of the inverter is verified in Fig. 35 and Fig. 36. Experiments are conducted under the full-load condition. Although three case meet IEEE Std 519-2014 harmonic current limits, either the PR current controller or the PIR current controller has lower harmonic contents than the PI current controller.



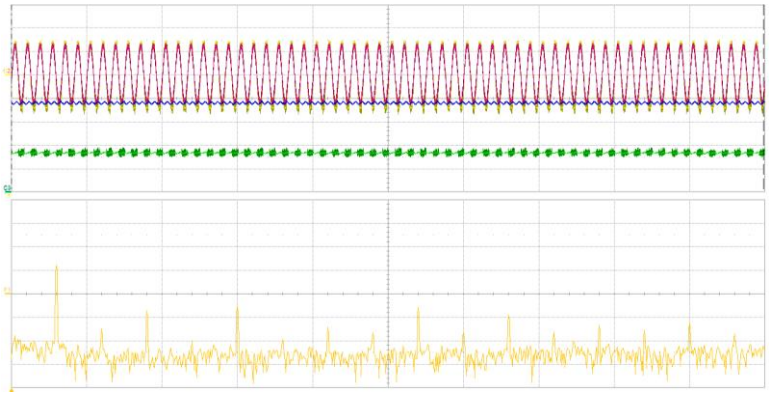
Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div FFT 20 dB/div

(a)



Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div FFT 20 dB/div

(b)



Grid voltage 200 V/div Inductor current 20 A/div Dc link voltage 100 V/div Dc side current 5 A/div Time 100 ms/div FFT 20 dB/div

(c)

Fig. 35. Experimental results of harmonics under full-load condition (a) PI current controller (b) PR current controller (c) PIR current controller

Fig. 36. Harmonic current distortion

Fig. 37 shows the efficiency of the inverter under various load conditions. When the PR controller and the PIR controller are used for current control, the inverter is slightly more efficient then when the PI current controller is adopted. These results come from harmonic contents. Harmonics lower the efficiency by inducing larger cable losses and instantaneous power fluctuation [13]. Thus, even if system meets the regulation for harmonics, it is necessary to reduce harmonics in order to improve the efficiency.

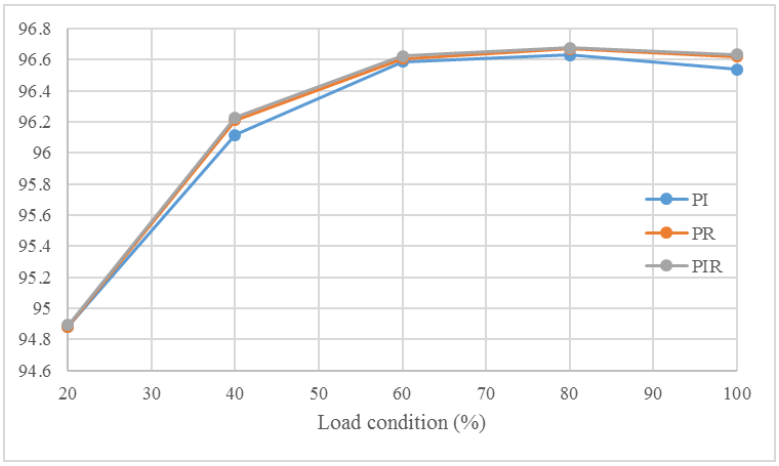


Fig. 37. Efficiency

V. CONCLUSION

In this thesis, the small-signal model of the single-phase grid-connected inverter is developed. The derived mathematical equations are verified by ac sweep simulation results. Based on theoretical model, stability and dynamics of the inverter system are investigated. The inverter is required to control the inductor current and the dc link voltage. Controllers are designed based on the small-signal model. In this thesis, it is proposed that the PIR controller is introduced to control the inductor current for the single-phase inverter. The PIR controller has not only harmonic suppression capability but also steady-state error elimination capability in single-phase inverter applications. The PIR controller is designed considering the phase margin and the crossover frequency of the current loop. In addition, the voltage controller is designed to regulate the dc link voltage. The proposed small-signal model and controllers are verified by simulations and experiments. The accuracy of small-signal model and the asymptotic approximation is evaluated by the dc link voltage with the step change in the dc side current. In addition, stability and dynamics of the inverter is investigated by transient behavior of the dc link voltage and the inductor current.

The steady-state error of the VSI is needed to be verified by experiments and further investigated. Then, the ability to eliminate the steady-state error generated by step change can be evaluated.

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